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PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-150664

(43)Date of publication of application : 30.05.2000

(51)Int.Cl.

H01L 21/8234

H01L 27/088

H01L 27/04

H01L 21/822

H01L 21/8238

H01L 27/092

H01L 29/78

H01L 29/786

(21)Application number : 10-324609

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(22)Date of filing : 16.11.1998

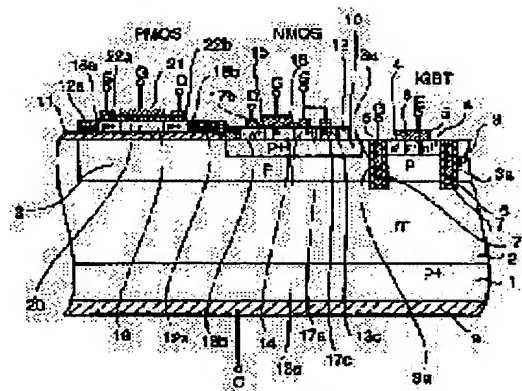
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(54) HIGH BREAKDOWN STRENGTH SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a highly reliable high breakdown strength semiconductor device at a low cost in which a high breakdown strength element and a drive circuit or a protection circuit, etc., are formed integrally.

SOLUTION: This semiconductor device is provided with an n-type MOS semiconductor element which is provided with a source layer 13a, a drain layer 13b, a gate insulation film 15, and a gate electrode 15 formed on an epitaxial single crystal semiconductor layer 10 on the surface of a semiconductor substrate, a p-type second MOS semiconductor element which is provided with a source layer 18a, a drain layer 18b, a gate insulation film 20, and a gate electrode 21 formed on a polycrystalline semiconductor layer that is piled up on the semiconductor substrate with an insulation film 11 interposed, and a high breakdown strength semiconductor element such as an IGBT(insulated gate bipolar transistor), etc., formed on the semiconductor substrate.



LEGAL STATUS

[Date of request for examination]

02.11.2004

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

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[Date of registration]

[Number of appeal against examiner's decision
of rejection]

[Date of requesting appeal against examiner's
decision of rejection]

[Date of extinction of right]

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CLAIMS

[Claim(s)]

[Claim 1] The 1st source layer and the 1st drain layer which were formed in the semi-conductor substrate front face, The 1st MOS mold semiconductor device of n mold which has the 1st gate electrode formed in said semi-conductor substrate front face between the 1st source layer concerned and the 1st drain layer through the 1st gate dielectric film, The 2nd source layer and the 2nd drain layer which were formed in the polycrystal semi-conductor layer by which the laminating was carried out through the insulator layer on said semi-conductor substrate, The 2nd MOS mold semiconductor device of p mold which has the 2nd gate electrode formed in said polycrystal semi-conductor layer front face between the 2nd source layer concerned and the 2nd drain layer through the 2nd gate dielectric film, The high proof-pressure semiconductor device characterized by providing the high proof-pressure semiconductor device formed in said semi-conductor substrate.

[Claim 2] The base layer of n mold with which said high proof-pressure semiconductor device was formed in said semi-conductor substrate, The 3rd source layer of n mold formed in the front face of the base layer of p mold formed in the front face of this n type of base layer, and this p type of base layer, and the contact layer of p mold, The 3rd gate electrode formed in the front face of said p type of base layer through the 3rd gate dielectric film, The 3rd drain layer formed in the location distant from said p type of base layer among the front faces of said n type of base layer, The high proof-pressure semiconductor device according to claim 1 characterized by having the 1st contact electrode which touches said 3rd source layer and said p type of contact layer, and the 2nd contact electrode which touches said 3rd drain layer.

[Claim 3] Said 1st source layer and the 1st drain layer are a high proof-pressure semiconductor device according to claim 2 characterized by being formed in the front face of said p type of base layer.

[Claim 4] The high proof-pressure semiconductor device according to claim 3 characterized by forming the semi-conductor layer of high-concentration p mold rather than the p type concerned of base layer between said 1st source layer and the 1st drain layer, and said p type of base layer.

[Claim 5] The 1st source layer and the 1st drain layer which were formed in the semi-conductor substrate front face at the epitaxial single crystal half conductor layer by which the laminating was carried out, The 1st MOS mold semiconductor device of n mold which has the 1st gate electrode formed in said semi-conductor substrate front face between the 1st source layer concerned and the 1st drain layer through the 1st gate dielectric film, The 2nd source layer and the 2nd drain layer which were formed in the polycrystal semi-conductor layer by which the laminating was carried out through the insulator layer on said semi-conductor substrate, The 2nd MOS mold semiconductor device of p mold which has the 2nd gate electrode formed in said polycrystal semi-conductor layer front face between the 2nd source layer concerned and the 2nd drain layer through the 2nd gate dielectric film, The high proof-pressure semiconductor device characterized by providing the high proof-pressure semiconductor device formed in said semi-conductor substrate.

[Claim 6] The base layer of n mold with which said high proof-pressure semiconductor device

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was formed in said semi-conductor substrate, The 3rd source layer of n mold formed in the front face of the base layer of p mold formed in the front face of this n type of base layer, and this p type of base layer, and the contact layer of p mold, The 3rd gate electrode formed in the front face of said p type of base layer through the 3rd gate dielectric film, The 3rd drain layer formed in the location distant from said p type of base layer among the front faces of said n type of base layer, The high proof-pressure semiconductor device according to claim 5 characterized by having the 1st contact electrode which touches said 3rd source layer and said p type of contact layer, and the 2nd contact electrode which touches said 3rd drain layer.

[Claim 7] Said epitaxial single crystal half conductor layer is a high proof-pressure semiconductor device according to claim 6 characterized by being formed in the front face of said p type of base layer.

[Claim 8] The high proof-pressure semiconductor device according to claim 7 characterized by forming the semi-conductor layer of high-concentration p mold rather than the p type concerned of base layer between said 1st source layer and the 1st drain layer, and said p type of base layer.

[Claim 9] The 1st source layer and the 1st drain layer which the insulator layer was formed on the semi-conductor substrate, and were formed in the semi-conductor layer which grew epitaxially ranging from said semi-conductor substrate front face to said insulator layer top, The 1st MOS mold semiconductor device of n mold which has the 1st gate electrode formed in said semi-conductor layer front face between the 1st source layer concerned and the 1st drain layer through the 1st gate dielectric film, The 2nd source layer and the 2nd drain layer which were formed in the part on said insulator layer of said semi-conductor layer, The 2nd MOS mold semiconductor device of p mold which has the 2nd gate electrode formed in said semi-conductor layer front face between this 2nd source layer and the 2nd drain layer through the 2nd gate dielectric film, The high proof-pressure semiconductor device characterized by providing the high proof-pressure semiconductor device formed in said semi-conductor substrate.

[Claim 10] It is the high proof-pressure semiconductor device according to claim 9 characterized by forming the 1st source layer of said 1st MOS mold semiconductor device in the part of said semi-conductor substrate front face of said epitaxially grown semi-conductor layer, and forming the 1st drain layer of the component concerned in the part on said insulator layer of said semi-conductor layer, respectively.

[Claim 11] The base layer of n mold with which said high proof-pressure semiconductor device was formed in said semi-conductor substrate, The 3rd source layer of n mold formed in the front face of the base layer of p mold formed in the front face of this n type of base layer, and this p type of base layer, and the contact layer of p mold, The 3rd gate electrode formed in the front face of said p type of base layer through the 3rd gate dielectric film, The 3rd drain layer formed in the location distant from said p type of base layer among the front faces of said n type of base layer, The high proof-pressure semiconductor device according to claim 9 or 10 characterized by having the 1st contact electrode which touches said 3rd source layer and said p type of contact layer, and the 2nd contact electrode which touches said 3rd drain layer.

[Claim 12] The part in which said 1st source layer of said epitaxially grown semi-conductor layer was formed is a high proof-pressure semiconductor device according to claim 11 characterized by being formed in the front face of said p type of base layer.

[Claim 13] The high proof-pressure semiconductor device according to claim 12 characterized by forming the semi-conductor layer of high-concentration p mold rather than the p type concerned of base layer between said 1st source layer and said p type of base layers.

[Claim 14] It is the high proof-pressure semiconductor device according to claim 9 to 13 characterized by for said epitaxially grown semi-conductor layer consisting of a single crystal, and the part on said insulator layer of said semi-conductor layer consisting of polycrystal.

[Claim 15] Said 3rd drain layer is a high proof-pressure semiconductor device claim 2 characterized by being p type layer 4 and 6 thru/or 8 or 11 thru/or given in 14.

[Claim 16] It is a high proof-pressure semiconductor device claim 2 characterized by for said high proof-pressure semiconductor device being a semiconductor device of a vertical mold, and forming said 3rd drain layer in the front face of said n type of the opposite side of base layer to

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said 3rd source layer 4 and 6 8 and 11 thru/or given in 15.

[Claim 17] Claim 2 characterized by forming a slot so that it may pierce through said 3rd source layer and said p type of base layer and said n type of base layer may be reached, and embedding said 3rd gate electrode through said 3rd gate dielectric film into this slot 4 and 6 8 and 11 thru/or a high proof-pressure semiconductor device given in 16.

[Claim 18] Claim 2 characterized by forming the semi-conductor layer of high-concentration n mold rather than the n type concerned of base layer between said n type of base layer, and said 3rd drain layer 4 and 6 8 and 11 thru/or a high proof-pressure semiconductor device given in 17.

[Claim 19] Said n type of 1st MOS mold semiconductor device and said p type of 2nd MOS mold semiconductor device are a high proof-pressure semiconductor device according to claim 1 to 18 characterized by constituting a CMOS circuit.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] Especially this invention relates to the high proof-pressure vertical mold semiconductor device which has an MOS mold semiconductor device with respect to a high proof-pressure semiconductor device.

[0002]

[Description of the Prior Art] High proof-pressure components, such as IGBT (Insulated Gate Bipolar Transistor), are used in many industrial fields, such as motor control and a power source. In order that this high proof-pressure component may treat large power, many vertical mold components which use the front face and rear face of a silicon substrate as a cathode, an anode or an emitter, and a collector are used.

[0003] In order to make easy to use a high proof-pressure component, especially vertical mold components, such as such IGBT, a drive circuit and a protection network are made to unify, and being hard to break and high-performance-izing a high proof-pressure component is performed. Usually, such a circuit is made apart from the chip of high proof-pressure components, such as IGBT, and the gestalt of the module of carrying in the same package is taken.

[0004] Although it became advantageous by leaps and bounds in respect of cost and dependability when these circuits could be carried on the same chip, there was no means to attain this easily with the conventional technique. For example, since the carrier plasma exists in the interior of IGBT when made on the same chip, a drive circuit, a protection network, for example, a CMOS circuit etc., etc., there is a problem that n mold MOS transistor (it is hereafter called NMOS for short.) and p mold MOS transistor (it is hereafter called PMOS for short.) will carry out a latch rise simply.

[0005] Moreover, in order to solve the above-mentioned problem, a polish recon layer is formed through an insulator layer on IGBT prepared in the semi-conductor substrate, and there is a high proof-pressure semiconductor device which prepared the CMOS circuit in this polish recon layer. Drawing 6 is the sectional view showing the structure of this high proof-pressure semiconductor device.

[0006] As shown in drawing 6, this high proof-pressure semiconductor device is a trench gate mold vertical mold quantity proof-pressure semiconductor device. n mold base layer 2 of high resistance is formed in the semi-conductor substrate, and high-concentration p mold drain layer 1 is formed in the whole surface of this n mold base layer 2. The drain electrode 9 is in contact with p mold drain layer 1. Moreover, p mold base layer 3 is formed in the field of another side of n mold base layer 2, and high-concentration n mold source layer 4 and high-concentration p mold contact layer 5 are formed in the front face of this p mold base layer 3.

[0007] Furthermore, two or more trench 3a is formed in the above-mentioned semi-conductor substrate front face. Such trench 3a is mutually arranged in parallel in the stripe-like top-face configuration (not shown), and it is formed so that n mold source layer 4 and p mold base layer 3 may be penetrated and n mold base layer 2 may be reached. In two or more trench 3a, the gate electrode 7 is embedded through gate dielectric film 6.

[0008] The above-mentioned n mold source layer 4 is formed in the field of the semi-conductor

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substrate front face between two or more trench 3a in contact with gate dielectric film 6, and as it is surrounded by n mold source layer 4, p mold contact layer 5 is formed so that clearly [drawing 6]. Moreover, in contact with n mold source layer 4 and p mold contact layer 5, the source electrode 8 is in contact.

[0009] As mentioned above, the trench gate mold vertical mold IGBT is formed in the semi-conductor substrate as a high proof-pressure semiconductor device, and the CMOS mold semiconductor device described below is formed on the same chip as this high proof-pressure semiconductor device.

[0010] That is, on p mold-base layer 3, the polycrystal (Pori) silicon layer 122 is formed through an insulator layer 121, NMOS and PMOS are formed in this polish recon layer 122, and NMOS and PMOS are further divided into each other by isolation insulator layer 122a.

[0011] NMOS consists of source electrode 105a and drain electrode 105b which contact source layer 101a formed in the polish recon layer 122 and drain layer 101b, the channel field 102 formed among these, the gate electrode 104 formed through the gate insulating layer 103 on this, source layer 101a, and drain layer 101b, respectively.

[0012] On the other hand, PMOS consists of source electrode 115a and drain electrode 115b which contact source layer 111a formed in the polish recon layer 122 and drain layer 111b, the channel field 112 formed among these, the gate electrode 114 formed through the gate insulating layer 113 on this, source layer 111a, and drain layer 111b, respectively.

[0013] IGBT and a CMOS circuit can be once carried on the same chip as mentioned above. However, the problem that a property is bad and cannot construct a highly precise analog circuit produces the CMOS semiconductor device formed in the polish recon layer prepared on the semi-conductor substrate.

[0014] That is, although a property with comparatively good PMOS formed in the polish recon layer is acquired, NMOS similarly formed in the polish recon layer has low channel mobility compared with NMOS formed in the single-crystal-silicon layer, and saturation characteristics are not acquired, either. Drawing 7 is the property Fig. showing the relation of the electrical potential difference between source drains of NMOS and PMOS (axis of abscissa) and drain current (axis of ordinate) which were formed in the polish recon layer. It turns out that drawing 7 (a) shows the property in the case of NMOS, a drain current also increases it by the increment in the electrical potential difference between source drains, and saturation characteristics are not acquired. On the other hand, although drawing 7 (b) shows the property in the case of PMOS and a drain current also increases it by the increment in the electrical potential difference between source drains, it turns out that saturation characteristics are acquired.

[0015]

[Problem(s) to be Solved by the Invention] the high proof-pressure component which was made to unify a drive circuit and a protection network in order to make a high proof-pressure component easy to use, could not break easily, and was high-performance-ized as stated above — dependability — although to provide by low cost highly was tried, there was no means to attain this easily with the conventional technique.

[0016] For example, since the carrier plasma exists in the interior of IGBT when made on the same chip, a drive circuit, a protection network, for example, a CMOS circuit etc., etc., there is a problem that NMOS and PMOS will carry out a latch rise simply.

[0017] Moreover, the problem that a property is bad and cannot construct a highly precise analog circuit produces the CMOS semiconductor device formed in the polish recon layer prepared on the semi-conductor substrate. the high proof-pressure semiconductor device which this invention was made in view of the above-mentioned actual condition, and unified the high proof-pressure component and the drive circuit, the protection network, etc. — dependability — it aims at providing by low cost highly.

[0018]

[Means for Solving the Problem] In order to solve the technical problem mentioned above, the 1st of this invention The 1st source layer and the 1st drain layer which were formed in the semi-conductor substrate front face, The 1st MOS mold semiconductor device of n mold which has the 1st gate electrode formed in said semi-conductor substrate front face between the 1st

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source layer concerned and the 1st drain layer through the 1st gate dielectric film, The 2nd source layer and the 2nd drain layer which were formed in the polycrystal semi-conductor layer by which the laminating was carried out through the insulator layer on said semi-conductor substrate, The 2nd MOS mold semiconductor device of p mold which has the 2nd gate electrode formed in said polycrystal semi-conductor layer front face between the 2nd source layer concerned and the 2nd drain layer through the 2nd gate dielectric film, The high proof-pressure semiconductor device characterized by providing the high proof-pressure semiconductor device formed in said semi-conductor substrate is offered.

[0019] Moreover, the 1st source layer and the 1st drain layer by which the 2nd of this invention was formed in the semi-conductor substrate front face at the epitaxial single crystal half conductor layer by which the laminating was carried out, The 1st MOS mold semiconductor device of n mold which has the 1st gate electrode formed in said semi-conductor substrate front face between the 1st source layer concerned and the 1st drain layer through the 1st gate dielectric film, The 2nd source layer and the 2nd drain layer which were formed in the polycrystal semi-conductor layer by which the laminating was carried out through the insulator layer on said semi-conductor substrate, The 2nd MOS mold semiconductor device of p mold which has the 2nd gate electrode formed in said polycrystal semi-conductor layer front face between the 2nd source layer concerned and the 2nd drain layer through the 2nd gate dielectric film, The high proof-pressure semiconductor device characterized by providing the high proof-pressure semiconductor device formed in said semi-conductor substrate is offered.

[0020] Moreover, the 1st source layer and the 1st drain layer which, as for the 3rd of this invention, the insulator layer was formed on the semi-conductor substrate, and were formed in the semi-conductor layer which grew epitaxially ranging from said semi-conductor substrate front face to said insulator layer top, The 1st MOS mold semiconductor device of n mold which has the 1st gate electrode formed in said semi-conductor layer front face between the 1st source layer concerned and the 1st drain layer through the 1st gate dielectric film, The 2nd source layer and the 2nd drain layer which were formed in the part on said insulator layer of said semi-conductor layer, The 2nd MOS mold semiconductor device of p mold which has the 2nd gate electrode formed in said semi-conductor layer front face between this 2nd source layer and the 2nd drain layer through the 2nd gate dielectric film, The high proof-pressure semiconductor device characterized by providing the high proof-pressure semiconductor device formed in said semi-conductor substrate is offered.

[0021] In above-mentioned this invention, it is desirable to provide the following configurations. In the 1st of this invention, and 2 and 3 (1) Said high proof-pressure semiconductor device The base layer of n mold formed in said semi-conductor substrate, and the base layer of p mold formed in the front face of this n type of base layer, The 3rd source layer of n mold formed in the front face of this p type of base layer, and the contact layer of p mold, The 3rd gate electrode formed in the front face of said p type of base layer through the 3rd gate dielectric film, Have the 1st contact electrode which touches the 3rd drain layer formed in the location distant from said p type of base layer among the front faces of said n type of base layer, said 3rd source layer, and said p type of contact layer, and the 2nd contact electrode which touches said 3rd drain layer.

[0022] (2) In the 1st of this invention, and 2 and 3, said 3rd drain layer should be p type layer. (3) Said high proof-pressure semiconductor device is a semiconductor device of a vertical mold, and said 3rd drain layer should be formed in the front face of said n type of the opposite side of base layer to said 3rd source layer in the 1st of this invention, and 2 and 3.

[0023] (4) A slot should be formed to pierce through said 3rd source layer and said p type of base layer, and to reach said n type of base layer, and said 3rd gate electrode should be embedded through said 3rd gate dielectric film in the 1st of this invention, and 2 and 3 in this slot.

[0024] (5) In the 1st of this invention, and 2 and 3, the semi-conductor layer of high-concentration n mold should be formed rather than the n type concerned of base layer between said n type of base layer, and said 3rd drain layer.

[0025] (6) this invention -- the -- one -- two -- three -- setting -- said -- n -- a mold -- the

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— one — MOS — a mold — a semiconductor device — said — p — a mold — the — two — MOS — a mold — a semiconductor device — a CMOS circuit — constituting — things — (— seven —) — this invention — the — one — setting — said — the — one — the source — a layer — and — the — one — a drain — a layer — said — p — a mold — the base — a layer — a front face — forming — having — **** .

[0026] (8) In the 2nd of this invention, said epitaxial single crystal half conductor layer should be formed in the front face of said p type of base layer.

(9) In the 1st of this invention, and 2, the semi-conductor layer of high-concentration p mold should be formed rather than the p type concerned of base layer between said 1st source layer and the 1st drain layer, and said p type of base layer.

[0027] (10) In the 3rd of this invention, the 1st source layer of said 1st MOS mold semiconductor device should be formed in the part of said semi-conductor substrate front face of said epitaxially grown semi-conductor layer, and the 1st drain layer of the component concerned should be formed in the part on said insulator layer of said semi-conductor layer, respectively.

[0028] (11) In the 3rd of this invention, the part in which said 1st source layer of said epitaxially grown semi-conductor layer was formed should be formed in the front face of said p type of base layer.

[0029] (12) In the 3rd of this invention, the semi-conductor layer of high-concentration p mold should be formed rather than the p type concerned of base layer between said 1st source layer and said p type of base layers.

[0030] (13) In the 3rd of this invention, said epitaxially grown semi-conductor layer should consist of a single crystal, and the part on said insulator layer of said semi-conductor layer should consist of polycrystal. In this invention, NMOS is formed in the epitaxial crystal layer prepared on the same silicon substrate as high proof-pressure semiconductor devices, such as IGBT, or this, for example, and PMOS is prepared on the polish recon layer prepared on the oxide film.

[0031] Although a property with comparatively good PMOS formed in the polish recon layer is acquired, when NMOS is formed in a polish recon layer, compared with what was formed in single crystal silicon, channel mobility is low, and saturation characteristics are not acquired, either. According to this invention, since IGBT etc. has p base diffusion layer, it can form NMOS comparatively easily into this p base diffusion layer like especially the 1st of this invention. According to this configuration, it is possible to acquire a good NMOS property.

[0032] Since leakage current may become large with this configuration for the plasma which exists in the interior, such as IGBT, the configuration shown below is more desirable. That is, it is desirable to prepare a short electrode between p bases and the sources concerned so that p base potential of NMOS may become the same as the source potential of high proof-pressure semiconductor devices, such as IGBT.

[0033] Moreover, in the 2nd of this invention, and the 3rd, it is possible to use the approach of preparing a silicon oxide pattern on a silicon substrate, applying on this silicon oxide pattern from on p base, preparing an amorphous silicon layer for example, annealing this at about 600 degrees C, and crystallizing. By this approach, an epitaxial growth silicon layer is formed on the above-mentioned p base, NMOS can be produced in this layer, and a polish recon layer is formed on the above-mentioned silicon oxide pattern, and PMOS can be produced in this layer. Consequently, PMOS formed in this polish recon layer and NMOS formed in the epitaxial growth silicon layer become possible [acquiring a good property also for ** in channel mobility and saturation characteristics].

[0034] A part of amorphous silicon layer made to extend on the above-mentioned silicon oxide pattern further again can also be considered as the epitaxial growth phase of a single crystal in the part near the above-mentioned p base. Therefore, it is possible to form the drain of NMOS, a channel (base), or the source in this part. For example, a channel (base) is formed in the single crystal epitaxial growth phase on a silicon oxide pattern, and the source of NMOS forms a drain in the epitaxial growth phase on p base at the epitaxial growth phase on the oxide-film pattern concerned (a single crystal or polish recon).

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[0035] According to this configuration, a good property can be acquired in channel mobility and saturation characteristics, and increase of leakage current can be prevented. Furthermore, since a drain exists on a silicon oxide pattern, it is possible to be able to prevent that a parasitic thyristor is constituted and to control thyristor actuation of a component by p mold drain layer of IGBT prepared in the silicon substrate, the high resistance n type layer, p mold base layer, and n mold source layer of NMOS.

[0036] As mentioned above, if this invention is caused, since NMOS will be prepared in a semiconductor substrate or the epitaxial growth phase on it and PMOS will be prepared in the polycrystal layer on an insulator layer, good NMOS and a PMOS property can be acquired and it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with high proof-pressure semiconductor devices, such as IGBT.

[0037]

[Embodiment of the Invention] It explains to a detail, using a drawing hereafter about the operation gestalt concerning the high proof-pressure semiconductor device of this invention. (1st operation gestalt) Drawing 1 is the sectional view showing the high proof-pressure semiconductor device concerning the 1st operation gestalt of this invention. The high proof-pressure semiconductor device of this operation gestalt is the trench gate mold vertical mold IGBT.

[0038] as shown in drawing 1, n mold base layer 2 of high resistance forms in a semiconductor substrate (silicon substrate) — having — **** — p+ of high concentration [whole surface / of this n mold base layer 2] The mold drain layer 1 is formed. The drain electrode 9 is in contact with p mold drain layer 1. moreover, p mold base layer 3 forms in the field of another side of n mold base layer 2 — having — **** — n+ of high concentration [front face / of this p mold base layer 3] The mold source layer 4 and high-concentration p+ The mold contact layer 5 is formed.

[0039] Furthermore, two or more trench 3a is formed in the above-mentioned semiconductor substrate front face. It is mutually arranged in parallel in the stripe-like top-face configuration (not shown), and such trench 3a is n+. It is formed so that the mold source layer 4 and p mold base layer 3 may be penetrated and n mold base layer 2 may be reached. In two or more trench 3a, the gate electrode 7 is embedded through gate dielectric film 6.

[0040] In the field of the semiconductor substrate front face between two or more trench 3a, it is above-mentioned n+ so that clearly [drawing 1]. The mold source layer 4 is formed in contact with gate dielectric film 6, and it is n+. It is p+ as it is surrounded by the mold source layer 4. The mold contact layer 5 is formed. Moreover, n+ mold source layer 4 and p+ In contact with the mold contact layer 5, the source electrode 8 is in contact. p+ Two or more arrangement may be carried out among trench 3a, and the mold contact layer 5 is n+. The mold source layer 4 and p+ It is the n+ concerned in order to take certainly contact of the source electrode 8 to the mold contact layer 5. The mold source layer 4 and p+ As for the mold contact layer 5, it is desirable to be arranged by turns along with the longitudinal direction of trench 1a.

[0041] As mentioned above, the trench gate mold vertical mold IGBT is formed in the semiconductor substrate as a high proof-pressure semiconductor device, and the CMOS mold semiconductor device described below is formed on the same chip as this high proof-pressure semiconductor device.

[0042] Namely, p+ of high concentration [front face / of p mold base layer 3 / layer / 3 / concerned / p mold base] The mold diffusion layer 10 is formed and it is this p+. The epitaxial single-crystal-silicon layer 12 is formed on the mold diffusion layer 10. On the other hand, it is p+. The insulating-layer pattern 11 is formed in a different field from the mold diffusion layer 10, and the polycrystal (Pori) silicon layer is prepared on this insulating-layer pattern 11. NMOS is formed in the epitaxial single-crystal-silicon layer 12, PMOS is formed in the polish recon layer on the insulating-layer pattern 11, respectively, and NMOS and PMOS are divided into each other by isolation insulator layer 12a.

[0043] That is, NMOS is n+ formed in the epitaxial single-crystal-silicon layer 12. Source layer 13a and drain layer 13b of a mold, The channel field 14 formed among these, the gate electrode

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16 formed through the gate insulating layer 15 on this, and p⁺ adjoined and formed in source layer 13a. Contact layer 13c of a mold, It consists of source layer 13a, drain layer 13b and source electrode 17a that contacts contact layer 13c, respectively, drain electrode 17b, and contact electrode 17c. Source electrode 17a and contact electrode 17c are electrically connected to each other.

[0044] On the other hand, PMOS is n⁺ formed in the polish recon layer. It consists of source electrode 22a and drain electrode 22b which contact source layer 18a of a mold and drain layer 18b, the channel field 19 formed among these, the gate electrode 21 formed through the gate insulating layer 20 on this, source layer 18a, and drain layer 18b, respectively.

[0045] As mentioned above, in this operation gestalt, while forming the epitaxial single-crystal-silicon layer 12 on the silicon substrate in which IGBT was formed and forming NMOS in this crystal layer 12, PMOS is prepared on the polish recon layer formed on the oxide film 11.

Although a property with comparatively good PMOS formed in the polish recon layer is acquired, when NMOS is formed in a polish recon layer, compared with what was formed in single crystal silicon, channel mobility is low, and saturation characteristics are not acquired, either. However, according to this operation gestalt, good NMOS and good PMOS can be obtained in channel mobility and saturation characteristics, and increase of leakage current can be prevented.

[0046] Moreover, since NMOS is formed in the amorphous silicon layer 10 crystallized on p mold base layer 3, a threshold becomes proper. That is, although the surface concentration of p mold base layer of the usual IGBT may be too high for NMOS, if the amorphous silicon layer which is not doped is formed on p mold base layer, even if p mold impurity is spread in the crystallization amorphous silicon layer 10 from p mold base layer, the surface concentration of the p mold base layer concerned will become lower than that of p mold base layer of IGBT, and the threshold of NMOS will be rationalized.

[0047] It is p⁺ further again. p mold drain layer 1 of IGBT prepared in the silicon substrate since the mold diffusion layer 10 intervened between the silicon substrate and the epitaxial single-crystal-silicon layer 12, n mold base layer 2, p mold base layer 3, and n⁺ of NMOS. It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by source layer 13a of a mold or drain layer 13b.

[0048] Thus, according to this operation gestalt, since good NMOS and a PMOS property can be acquired, it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with IGBT.

[0049] The manufacture approach of the high proof-pressure semiconductor device by this operation gestalt described above is as stating below. first, trench 1a of a vertical mold IGBT — forming — preceding — the front face of p mold base layer 3 of a semi-conductor substrate — p⁺ the mold diffusion layer 10 — forming — this p⁺ the field except the mold diffusion layer 10 and an IGBT formation schedule field — alternative — an oxide film 11 — for example, LOCOS — it forms by law. After forming an oxide film 11, this oxide-film 11 grade is used as a mask here, and it is p⁺ by an ion implantation etc. The mold diffusion layer 10 may be formed.

[0050] Next, p⁺ of p mold base layer 3 front face. Apply on an oxide film 11 from the mold diffusion layer 10, and about 0.5 micrometers of amorphous silicon (a-Si) layers are made to deposit, at 600 degrees C, it anneals for about 20 hours and solid phase growth is carried out. It is p⁺ by this annealing. While single-crystal-izing the amorphous silicon layer on the mold diffusion layer 10 and becoming the epitaxial single-crystal-silicon layer 12, the amorphous silicon layer on an oxide film 11 turns into a polish recon layer.

[0051] Then, by the ion implantation, n mold impurity is introduced into the field to which PMOS of said polish recon layer is formed in the field in which NMOS of the epitaxial single-crystal-silicon layer 12 is formed in p mold impurity, respectively, and it considers as the p type semiconductor layer 14 and the n-type-semiconductor layer 19, respectively. Furthermore, isolation oxide-film 12a which divides these components into an oxidation part is formed by oxidizing the field except the field in which PMOS of the field in which NMOS of the epitaxial single-crystal-silicon layer 12 is formed, and said polish recon layer is formed.

[0052] Next, in order to form the gate of IGBT, trench 3a is formed in a silicon substrate. The gate oxide (15 20) of NMOS and PMOS is formed [the inside of trench 3a] in the front face of

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the epitaxial single-crystal-silicon layer 12 and the above-mentioned polish recon layer for gate oxide 6 at coincidence, respectively. Furthermore, the polish recon film is deposited so that a trench may be embedded on this, and the gate electrode 7 of IGBT is produced. This polish recon film is deposited also on the gate oxide (15 20) of NMOS and PMOS at coincidence, and can also form the gate electrode (16 21) of NMOS and PMOS.

[0053] next, the gate electrode 7 and a gate electrode (16 21) — a mask — carrying out — respectively — an ion implantation — n^+ of IGBT n^+ of the mold source layer 4 and NMOS mold source layer 13a and the drain layer 13 — p^+ of b and PMOS Mold source layer 18a and drain layer 18b are formed. Moreover, p^+ of IGBT p^+ of the mold contact layer 5 and NMOS Mold contact layer 13c is formed by the ion implantation.

[0054] Then, n^+ of IGBT The mold source layer 4 and p^+ The drain electrode 9 is formed in the source electrode 8 and p mold drain layer 1 at the mold contact layer 5. To source layer 13a of NMOS, drain layer 13b, and contact layer 13c, respectively Source electrode 17a, Drain electrode 17b and contact electrode 17c are formed, source electrode 22a and drain electrode 22b are formed in source layer 18a of PMOS, and drain layer 18b, respectively, and the high proof-pressure semiconductor device of this operation gestalt is completed.

[0055] (2nd operation gestalt) Drawing 2 is the sectional view showing the high proof-pressure semiconductor device concerning the 2nd operation gestalt of this invention. The same sign is attached and shown in the same part as drawing 1, and detailed explanation is omitted. The point that this operation gestalt differs from the 1st operation gestalt is a point that a part of epitaxial single-crystal-silicon layer is formed on an insulating-layer pattern, and the drain layer of NMOS and a part of channel field are formed in a part of this single-crystal-silicon layer.

[0056] As shown in drawing 2, the trench gate mold vertical mold IGBT is formed in the semiconductor substrate as a high proof-pressure semiconductor device, and the CMOS mold semiconductor device described below is formed on the same chip as this high proof-pressure semiconductor device.

[0057] That is, on a silicon substrate, the insulating-layer pattern 11 is formed alternatively, and on this insulating-layer pattern 11, as it runs aground in part, the epitaxial single-crystal-silicon layer 12 is formed on p mold base layer 3. Moreover, the polycrystal (Pori) silicon layer is prepared on the insulating-layer pattern 11. NMOS is formed in the epitaxial single-crystal-silicon layer 12, PMOS is formed in the polish recon layer on the insulating-layer pattern 11, respectively, and NMOS and PMOS are divided into each other by isolation insulator layer 12b.

[0058] That is, NMOS is n^+ formed in the epitaxial single-crystal-silicon layer 12. Source layer 31a and drain layer 31b of a mold, The channel field 32 formed among these, the gate electrode 34 formed through the gate insulating layer 33 on this, and p^+ adjoined and formed in source layer 31a Contact layer 31c of a mold, It consists of drain electrode 35b in contact with source electrode 35a in contact with source layer 31a and contact layer 31c, and drain layer 31b. A part of drain layer 31b of NMOS and channel field 32 are formed in a part of epitaxial single-crystal-silicon layer 12 on the insulating-layer pattern 11, and source layer 31a is formed in a part of epitaxial single-crystal-silicon layer 12 of p mold base layer 3 front face where the insulating-layer pattern 11 does not exist.

[0059] On the other hand, PMOS is n^+ formed in the polish recon layer. It consists of source electrode 45a and drain electrode 45b which contact source layer 41a of a mold and drain layer 41b, the channel field 42 formed among these, the gate electrode 44 formed through the gate insulating layer 43 on this, source layer 41a, and drain layer 41b, respectively.

[0060] According to this operation gestalt, in channel mobility and saturation characteristics, good NMOS and good PMOS can be obtained like the 1st operation gestalt, and increase of leakage current can be prevented. Moreover, it is also possible to rationalize the threshold of NMOS.

[0061] Also in this operation gestalt, like the 1st operation gestalt, it applies on the insulating-layer pattern 11 from p mold base layer 3 of a silicon substrate, and an amorphous silicon layer is formed, and this amorphous silicon layer is single-crystal-ized, using a silicon substrate as seed crystal. By this single crystal-ization, a part of part near seed crystal also single-crystal-izes the amorphous silicon layer on the insulating-layer pattern 11. By forming a part of channel

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field 32 of NMOS, and drain layer 31b in the part of this single-crystal-ized amorphous silicon layer, it is possible to prevent increase of the leakage current of NMOS certainly. Since especially the channel field 52 is close to the silicon substrate used as seed crystal, it is possible to acquire the crystallinity which may be set to the channel field 52, and the effectiveness of leakage current prevention is large. Furthermore, it is also possible to form in the polish recon field to which that point did not single-crystal-ize drain layer 31b for the channel field 32 of NMOS to the single crystal-ized field of an amorphous silicon layer, and increase of the leakage current of NMOS can be prevented also in this case.

[0062] p mold drain layer 1 of IGBT prepared in the silicon substrate further again since the insulating-layer pattern 11 intervened between the silicon substrate and the epitaxial single-crystal-silicon layer 12, n mold base layer 2, p mold base layer 3, and n⁺ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by drain layer 31b of a mold.

[0063] in addition, the 1st operation gestalt — the same — p⁺ of high concentration [front face / of p mold base layer 3 / layer / 3 / concerned / p mold base] a mold diffusion layer forms — having — this p⁺ The channel field 32, source layer 31a, and contact layer 31c may be made to be formed in the front face of a mold diffusion layer. p mold drain layer 1 of IGBT which this prepared in the silicon substrate like the 1st operation gestalt, n mold base layer 2, p mold base layer 3, and n⁺ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by source layer 31a of a mold.

[0064] Thus, according to this operation gestalt, since good NMOS and a PMOS property can be acquired, it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with IGBT.

[0065] (3rd operation gestalt) Drawing 3 is the sectional view showing the high proof-pressure semiconductor device concerning the 3rd operation gestalt of this invention. The same sign is attached and shown in the same part as drawing 2, and detailed explanation is omitted. The point that this operation gestalt differs from the 2nd operation gestalt is a point that the drain layer of NMOS, all of channel fields, and a part of source layer are formed in a part of epitaxial single-crystal-silicon layer formed on the insulating-layer pattern.

[0066] As shown in drawing 3, the trench gate mold vertical mold IGBT is formed in the semiconductor substrate as a high proof-pressure semiconductor device, and the CMOS mold semiconductor device described below is formed on the same chip as this high proof-pressure semiconductor device.

[0067] That is, on a silicon substrate, the insulating-layer pattern 11 is formed alternatively, and on this insulating-layer pattern 11, as it runs aground in part, the epitaxial single-crystal-silicon layer 12 is formed on p mold base layer 3. Moreover, on the insulating-layer pattern 11, 12f of polycrystal (Pori) silicon layers is prepared. NMOS is formed in the epitaxial single-crystal-silicon layer 12, PMOS (not shown) is formed in 12f of polish recon layers on the insulating-layer pattern 11, respectively, and NMOS and PMOS are divided into each other by isolation insulator layer 12c.

[0068] That is, NMOS is n⁺ formed in the epitaxial single-crystal-silicon layer 12. Source layer 51a and drain layer 51b of a mold, The channel field 52 formed among these, the gate electrode 54 formed through the gate insulating layer 53 on this, and p⁺ adjoined and formed in source layer 51a Contact layer 51c of a mold, It consists of drain electrode 55b in contact with source electrode 55a in contact with source layer 51a and contact layer 51c, and drain layer 51b. A part for drain layer 51b of NMOS and all of the channel fields 52 and a part of source layer 51a are formed in a part of epitaxial single-crystal-silicon layer 12 on the insulating-layer pattern 11, and a part of source layer 51a is formed in a part of epitaxial single-crystal-silicon layer 12 of p mold base layer 3 front face where the insulating-layer pattern 11 does not exist.

[0069] According to this operation gestalt, in channel mobility and saturation characteristics, good NMOS and good PMOS can be obtained like the 1st operation gestalt, and increase of leakage current can be prevented. Moreover, it is also possible to rationalize the threshold of NMOS.

[0070] Also in this operation gestalt, the amorphous silicon layer formed on the insulating-layer

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pattern 11 from p mold base layer 3 of a silicon substrate, having applied is single-crystal-ized like the 2nd operation gestalt, using a silicon substrate as seed crystal. When a part of part also with the amorphous silicon layer near seed crystal on the insulating-layer pattern 11 single-crystal-izes and forms a part for drain layer 51b of NMOS, and all of the channel fields 52, and a part of source layer 51a in the part of this single-crystal-ized amorphous silicon layer by this single crystal-ization, it is possible to prevent increase of the leakage current of NMOS certainly. Since especially the channel field 52 is close to the silicon substrate used as seed crystal, it is possible to acquire the crystallinity which may be set to the channel field 52, and the effectiveness of leakage current prevention is large. Furthermore, it is also possible to form in the polish recon field to which that point did not single-crystal-ize drain layer 51b for the channel field 52 of NMOS to the single crystal-ized field of an amorphous silicon layer, and increase of the leakage current of NMOS can be prevented also in this case. Moreover, since the channel field 52 of NMOS is completely insulated from the silicon substrate with this structure, as for this channel field 52, it is hard to be influenced of the potential of a silicon substrate, and a setup of a threshold and control become easy.

[0071] p mold drain layer 1 of IGBT prepared in the silicon substrate with the insulating-layer pattern 11 further again, n mold base layer 2, p mold base layer 3, and n⁺ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by drain layer 51b of a mold.

[0072] in addition, the 1st operation gestalt — the same — p⁺ of high concentration [front face / of p mold base layer 3 / layer / 3 / concerned / p mold base] a mold diffusion layer forms — having — this p⁺ Source layer 51a and contact layer 51c may be made to be formed in the front face of a mold diffusion layer. p mold drain layer 1 of IGBT which this prepared in the silicon substrate like the 1st operation gestalt, n mold base layer 2, p mold base layer 3, and n⁺ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by source layer 51a of a mold.

[0073] Thus, according to this operation gestalt, since good NMOS and a PMOS property can be acquired, it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with IGBT.

[0074] (4th operation gestalt) Drawing 4 is the sectional view showing the high proof-pressure semiconductor device concerning the 4th operation gestalt of this invention. The same sign is attached and shown in the same part as drawing 1 , and detailed explanation is omitted. The point that this operation gestalt differs from the 1st operation gestalt is a point that NMOS is formed in p mold base layer of IGBT of a silicon substrate, and high-concentration p type layer is formed between this NMOS and p mold base layer.

[0075] As shown in drawing 4 , the trench gate mold vertical mold IGBT is formed in the semiconductor substrate as a high proof-pressure semiconductor device, and the CMOS mold semiconductor device described below is formed on the same chip as this high proof-pressure semiconductor device.

[0076] That is, on a silicon substrate, the insulating-layer pattern 11 is formed alternatively, and 12g of polycrystal (Pori) silicon layers is prepared on this insulating-layer pattern 11. PMOS is formed in 12g of this polish recon layer. Moreover, rather than p mold base layer 3, low-concentration p type semiconductor layer 3b is formed alternatively, and NMOS is formed in the field in which NMOS in p mold base layer 3 is formed at this p type semiconductor layer 3b. NMOS and PMOS are divided into each other by 12d of isolation insulator layers.

[0077] That is, NMOS is n⁺ formed in p type semiconductor layer 3b. Source layer 61a and drain layer 61b of a mold, The channel field 62 formed among these, the gate electrode 64 formed through the gate insulating layer 63 on this, and p⁺ adjoined and formed in source layer 61a Contact layer 61c of a mold, It consists of drain electrode 65b in contact with source electrode 65a in contact with source layer 61a and contact layer 61c, and drain layer 61b. p⁺ of high concentration [b / under Above NMOS / p type semiconductor layer 3/ layer / 3 / p type semiconductor layer 3b / concerned / or / p mold base] Mold diffusion layer 3c is formed.

[0078] On the other hand, PMOS is n⁺ formed in 12g of polish recon layers. It consists of source electrode 75a and drain electrode 75b which contact source layer 71a of a mold and drain layer

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71b, the channel field 72 formed among these, the gate electrode 74 formed through the gate insulating layer 73 on this, source layer 71a, and drain layer 71b, respectively.

[0079] According to this operation gestalt, since NMOS is formed in p type semiconductor layer 3b of a silicon substrate, NMOS will be formed in the crystalline good single crystal part, good NMOS and good PMOS can be obtained in channel mobility and saturation characteristics like the 1st operation gestalt, and increase of leakage current can be prevented.

[0080] Moreover, since NMOS is formed in the low-concentration p type semiconductor layer 3 rather than p mold base layer 3 of IGBT, it is also possible to rationalize the threshold of the NMOS concerned. Formation of this p type semiconductor layer 3 is performed in advance of formation of p mold base layer of IGBT.

[0081] p+ of high concentration [layer / 3 / p type semiconductor layer 3b or / p mold base] further again p mold drain layer 1 of IGBT prepared in the silicon substrate by mold diffusion layer 3c, n mold base layer 2, p mold base layer 3, and n+ of NMOS. It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by source layer 61a of a mold or drain layer 61b.

[0082] Thus, according to this operation gestalt, since good NMOS and a PMOS property can be acquired, it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with IGBT.

[0083] (5th operation gestalt) Drawing 5 is the sectional view showing the high proof-pressure semiconductor device concerning the 5th operation gestalt of this invention. The same sign is attached and shown in the same part as drawing 4, and detailed explanation is omitted. The point that this operation gestalt differs from the 4th operation gestalt is a point that diode is formed in the polycrystal (Pori) silicon layer formed on the insulating-layer pattern.

[0084] As shown in drawing 5, the trench gate mold vertical mold IGBT is formed in the semiconductor substrate as a high proof-pressure semiconductor device, and the diode described below is formed on the same chip as this high proof-pressure semiconductor device.

[0085] That is, on a silicon substrate, the insulating-layer pattern 11 is formed alternatively, and the polycrystal (Pori) silicon layer is prepared on this insulating-layer pattern 11. Diode is formed in this polish recon layer. Moreover, rather than p mold base layer 3, low-concentration p type semiconductor layer 3b is formed alternatively, and NMOS is formed in the field in which NMOS in p mold base layer 3 is formed at this p type semiconductor layer 3b. NMOS and diode are divided into each other by isolation insulator layer 12e.

[0086] That is, NMOS is n+ formed in p type semiconductor layer 3b. Source layer 81a and drain layer 81b of a mold, The channel field 82 formed among these, the gate electrode 84 formed through the gate insulating layer 83 on this, and p+ adjoined and formed in source layer 81a. Contact layer 81c of a mold, It consists of drain electrode 85b in contact with source electrode 85a in contact with source layer 81a and contact layer 81c, and drain layer 81b. p+ of high concentration [b / under Above NMOS / p type semiconductor layer 3 / layer / 3 / p type semiconductor layer 3b / concerned / or / p mold base] Mold diffusion layer 3c is formed.

[0087] On the other hand, diode is p+ formed in the polish recon layer. Anode layer 91a of a mold, and n+ It consists of anode electrode 92a and cathode electrode 92b which contact cathode layer 91b of a mold, anode layer 91a, and cathode layer 91b, respectively.

[0088] According to this operation gestalt, in channel mobility and saturation characteristics, good NMOS can be obtained like the 4th operation gestalt, and increase of leakage current can be prevented.

[0089] Moreover, it is also possible to rationalize the threshold of NMOS by the p type semiconductor layer 3 like the 4th operation gestalt. Furthermore, p+ p mold drain layer 1 of IGBT prepared in the silicon substrate by mold diffusion layer 3c, n mold base layer 2, p mold base layer 3, and n+ of NMOS. It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by source layer 81a of a mold or drain layer 81b.

[0090] Thus, according to this operation gestalt, since a good NMOS property can be acquired, it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with IGBT.

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[0091] In addition, this invention is not limited to the above-mentioned operation gestalt. For example, p+ Between the mold drain layer 1 and n mold base layer 2, high-concentration n mold buffer layer can be formed rather than the n mold base layer 2 concerned, and it is possible to raise conductivity.

[0092] Moreover, although the above-mentioned operation gestalt explained the high proof-pressure semiconductor device of a vertical mold, this invention is applicable also to the high proof-pressure semiconductor device of a horizontal type. In this case, a drain layer is formed in the semi-conductor substrate front face of the same side as a source layer.

[0093] At the above-mentioned operation gestalt, it is p+ further again. It is a drain layer, although IGBT which has the drain layer of a mold was mentioned as the example and explained n+ It is also possible to consider as a mold and to apply to various quantity proof-pressure semiconductor devices, such as an MOS mold quantity proof-pressure semiconductor device and other thyristors. In addition, it is possible to deform variously and to carry out in the range which does not deviate from the meaning of this invention.

[0094]

[Effect of the Invention] the high proof-pressure semiconductor device which unified the high proof-pressure component and the drive circuit, the protection network, etc. according to this invention — dependability — it can provide by low cost highly.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] the high proof-pressure component which was made to unify a drive circuit and a protection network in order to make a high proof-pressure component easy to use, could not break easily, and was high-performance-ized as stated above -- dependability -- although to provide by low cost highly was tried, there was no means to attain this easily with the conventional technique.

[0016] For example, since the carrier plasma exists in the interior of IGBT when made on the same chip, a drive circuit, a protection network, for example, a CMOS circuit etc., etc., there is a problem that NMOS and PMOS will carry out a latch rise simply.

[0017] Moreover, the problem that a property is bad and cannot construct a highly precise analog circuit produces the CMOS semiconductor device formed in the polish recon layer prepared on the semi-conductor substrate. the high proof-pressure semiconductor device which this invention was made in view of the above-mentioned actual condition, and unified the high proof-pressure component and the drive circuit, the protection network, etc. -- dependability -- it aims at providing by low cost highly.

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MEANS

[Means for Solving the Problem] In order to solve the technical problem mentioned above, the 1st of this invention The 1st source layer and the 1st drain layer which were formed in the semi-conductor substrate front face, The 1st MOS mold semiconductor device of n mold which has the 1st gate electrode formed in said semi-conductor substrate front face between the 1st source layer concerned and the 1st drain layer through the 1st gate dielectric film, The 2nd source layer and the 2nd drain layer which were formed in the polycrystal semi-conductor layer by which the laminating was carried out through the insulator layer on said semi-conductor substrate, The 2nd MOS mold semiconductor device of p mold which has the 2nd gate electrode formed in said polycrystal semi-conductor layer front face between the 2nd source layer concerned and the 2nd drain layer through the 2nd gate dielectric film, The high proof-pressure semiconductor device characterized by providing the high proof-pressure semiconductor device formed in said semi-conductor substrate is offered.

[0019] Moreover, the 1st source layer and the 1st drain layer by which the 2nd of this invention was formed in the semi-conductor substrate front face at the epitaxial single crystal half conductor layer by which the laminating was carried out, The 1st MOS mold semiconductor device of n mold which has the 1st gate electrode formed in said semi-conductor substrate front face between the 1st source layer concerned and the 1st drain layer through the 1st gate dielectric film, The 2nd source layer and the 2nd drain layer which were formed in the polycrystal semi-conductor layer by which the laminating was carried out through the insulator layer on said semi-conductor substrate, The 2nd MOS mold semiconductor device of p mold which has the 2nd gate electrode formed in said polycrystal semi-conductor layer front face between the 2nd source layer concerned and the 2nd drain layer through the 2nd gate dielectric film, The high proof-pressure semiconductor device characterized by providing the high proof-pressure semiconductor device formed in said semi-conductor substrate is offered.

[0020] Moreover, the 1st source layer and the 1st drain layer which, as for the 3rd of this invention, the insulator layer was formed on the semi-conductor substrate, and were formed in the semi-conductor layer which grew epitaxially ranging from said semi-conductor substrate front face to said insulator layer top, The 1st MOS mold semiconductor device of n mold which has the 1st gate electrode formed in said semi-conductor layer front face between the 1st source layer concerned and the 1st drain layer through the 1st gate dielectric film, The 2nd source layer and the 2nd drain layer which were formed in the part on said insulator layer of said semi-conductor layer, The 2nd MOS mold semiconductor device of p mold which has the 2nd gate electrode formed in said semi-conductor layer front face between this 2nd source layer and the 2nd drain layer through the 2nd gate dielectric film, The high proof-pressure semiconductor device characterized by providing the high proof-pressure semiconductor device formed in said semi-conductor substrate is offered.

[0021] In above-mentioned this invention, it is desirable to provide the following configurations. In the 1st of this invention, and 2 and 3 (1) Said high proof-pressure semiconductor device The base layer of n mold formed in said semi-conductor substrate, and the base layer of p mold formed in the front face of this n type of base layer, The 3rd source layer of n mold formed in the front face of this p type of base layer, and the contact layer of p mold, The 3rd gate

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electrode formed in the front face of said p type of base layer through the 3rd gate dielectric film, Have the 1st contact electrode which touches the 3rd drain layer formed in the location distant from said p type of base layer among the front faces of said n type of base layer, said 3rd source layer, and said p type of contact layer, and the 2nd contact electrode which touches said 3rd drain layer.

[0022] (2) In the 1st of this invention, and 2 and 3, said 3rd drain layer should be p type layer.

(3) Said high proof-pressure semiconductor device is a semiconductor device of a vertical mold, and said 3rd drain layer should be formed in the front face of said n type of the opposite side of base layer to said 3rd source layer in the 1st of this invention, and 2 and 3.

[0023] (4) A slot should be formed to pierce through said 3rd source layer and said p type of base layer, and to reach said n type of base layer, and said 3rd gate electrode should be embedded through said 3rd gate dielectric film in the 1st of this invention, and 2 and 3 in this slot.

[0024] (5) In the 1st of this invention, and 2 and 3, the semi-conductor layer of high-concentration n mold should be formed rather than the n type concerned of base layer between said n type of base layer, and said 3rd drain layer.

[0025] (6) this invention -- the -- one -- two -- three -- setting -- said -- n -- a mold -- the -- one -- MOS -- a mold -- a semiconductor device -- said -- p -- a mold -- the -- two -- MOS -- a mold -- a semiconductor device -- a CMOS circuit -- constituting -- things -- (-- seven --) -- this invention -- the -- one -- setting -- said -- the -- one -- the source -- a layer -- and -- the -- one -- a drain -- a layer -- said -- p -- a mold -- the base -- a layer -- a front face -- forming -- having -- **** .

[0026] (8) In the 2nd of this invention, said epitaxial single crystal half conductor layer should be formed in the front face of said p type of base layer.

(9) In the 1st of this invention, and 2, the semi-conductor layer of high-concentration p mold should be formed rather than the p type concerned of base layer between said 1st source layer and the 1st drain layer, and said p type of base layer.

[0027] (10) In the 3rd of this invention, the 1st source layer of said 1st MOS mold semiconductor device should be formed in the part of said semi-conductor substrate front face of said epitaxially grown semi-conductor layer, and the 1st drain layer of the component concerned should be formed in the part on said insulator layer of said semi-conductor layer, respectively.

[0028] (11) In the 3rd of this invention, the part in which said 1st source layer of said epitaxially grown semi-conductor layer was formed should be formed in the front face of said p type of base layer.

[0029] (12) In the 3rd of this invention, the semi-conductor layer of high-concentration p mold should be formed rather than the p type concerned of base layer between said 1st source layer and said p type of base layers.

[0030] (13) In the 3rd of this invention, said epitaxially grown semi-conductor layer should consist of a single crystal, and the part on said insulator layer of said semi-conductor layer should consist of polycrystal. In this invention, NMOS is formed in the epitaxial crystal layer prepared on the same silicon substrate as high proof-pressure semiconductor devices, such as IGBT, or this, for example, and PMOS is prepared on the polish recon layer prepared on the oxide film.

[0031] Although a property with comparatively good PMOS formed in the polish recon layer is acquired, when NMOS is formed in a polish recon layer, compared with what was formed in single crystal silicon, channel mobility is low, and saturation characteristics are not acquired, either. According to this invention, since IGBT etc. has p base diffusion layer, it can form NMOS comparatively easily into this p base diffusion layer like especially the 1st of this invention. According to this configuration, it is possible to acquire a good NMOS property.

[0032] Since leakage current may become large with this configuration for the plasma which exists in the interior, such as IGBT, the configuration shown below is more desirable. That is, it is desirable to prepare a short electrode between p bases and the sources concerned so that p base potential of NMOS may become the same as the source potential of high proof-pressure

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semiconductor devices, such as IGBT.

[0033] Moreover, in the 2nd of this invention, and the 3rd, it is possible to use the approach of preparing a silicon oxide pattern on a silicon substrate, applying on this silicon oxide pattern from on p base, preparing an amorphous silicon layer for example, annealing this at about 600 degrees C, and crystallizing. By this approach, an epitaxial growth silicon layer is formed on the above-mentioned p base, NMOS can be produced in this layer, and a polish recon layer is formed on the above-mentioned silicon oxide pattern, and PMOS can be produced in this layer. Consequently, PMOS formed in this polish recon layer and NMOS formed in the epitaxial growth silicon layer become possible [acquiring a good property also for ** in channel mobility and saturation characteristics].

[0034] A part of amorphous silicon layer made to extend on the above-mentioned silicon oxide pattern further again can also be considered as the epitaxial growth phase of a single crystal in the part near the above-mentioned p base. Therefore, it is possible to form the drain of NMOS, a channel (base), or the source in this part. For example, a channel (base) is formed in the single crystal epitaxial growth phase on a silicon oxide pattern, and the source of NMOS forms a drain in the epitaxial growth phase on p base at the epitaxial growth phase on the oxide-film pattern concerned (a single crystal or polish recon).

[0035] According to this configuration, a good property can be acquired in channel mobility and saturation characteristics, and increase of leakage current can be prevented. Furthermore, since a drain exists on a silicon oxide pattern, it is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by p mold drain layer of IGBT prepared in the silicon substrate, the high resistance n type layer, p mold base layer, and n mold source layer of NMOS.

[0036] As mentioned above, if this invention is caused, since NMOS will be prepared in a semiconductor substrate or the epitaxial growth phase on it and PMOS will be prepared in the polycrystal layer on an insulator layer, good NMOS and a PMOS property can be acquired and it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with high proof-pressure semiconductor devices, such as IGBT.

[0037]

[Embodiment of the Invention] It explains to a detail, using a drawing hereafter about the operation gestalt concerning the high proof-pressure semiconductor device of this invention. (1st operation gestalt) Drawing 1 is the sectional view showing the high proof-pressure semiconductor device concerning the 1st operation gestalt of this invention. The high proof-pressure semiconductor device of this operation gestalt is the trench gate mold vertical mold IGBT.

[0038] as shown in drawing 1 , n mold base layer 2 of high resistance forms in a semi-conductor substrate (silicon substrate) — having — **** — p+ of high concentration [whole surface / of this n mold base layer 2] The mold drain layer 1 is formed. The drain electrode 9 is in contact with p mold drain layer 1. moreover, p mold base layer 3 forms in the field of another side of n mold base layer 2 — having — **** — n+ of high concentration [front face / of this p mold base layer 3] The mold source layer 4 and high-concentration p+ The mold contact layer 5 is formed.

[0039] Furthermore, two or more trench 3a is formed in the above-mentioned semi-conductor substrate front face. It is mutually arranged in parallel in the stripe-like top-face configuration (not shown), and such trench 3a is n+. It is formed so that the mold source layer 4 and p mold base layer 3 may be penetrated and n mold base layer 2 may be reached. In two or more trench 3a, the gate electrode 7 is embedded through gate dielectric film 6.

[0040] In the field of the semi-conductor substrate front face between two or more trench 3a, it is above-mentioned n+ so that clearly [drawing 1]. The mold source layer 4 is formed in contact with gate dielectric film 6, and it is n+. It is p+ as it is surrounded by the mold source layer 4. The mold contact layer 5 is formed. Moreover, n+ mold source layer 4 and p+ In contact with the mold contact layer 5, the source electrode 8 is in contact. p+ Two or more arrangement may be carried out among trench 3a, and the mold contact layer 5 is n+. The mold source layer 4

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and p+ It is the n+ concerned in order to take certainly contact of the source electrode 8 to the mold contact layer 5. The mold source layer 4 and p+ As for the mold contact layer 5, it is desirable to be arranged by turns along with the longitudinal direction of trench 1a.

[0041] As mentioned above, the trench gate mold vertical mold IGBT is formed in the semiconductor substrate as a high proof-pressure semiconductor device, and the CMOS mold semiconductor device described below is formed on the same chip as this high proof-pressure semiconductor device.

[0042] Namely, p+ of high concentration [front face / of p mold base layer 3 / layer / 3 / concerned / p mold base] The mold diffusion layer 10 is formed and it is this p+. The epitaxial single-crystal-silicon layer 12 is formed on the mold diffusion layer 10. On the other hand, it is p+. The insulating-layer pattern 11 is formed in a different field from the mold diffusion layer 10, and the polycrystal (Pori) silicon layer is prepared on this insulating-layer pattern 11. NMOS is formed in the epitaxial single-crystal-silicon layer 12, PMOS is formed in the polish recon layer on the insulating-layer pattern 11, respectively, and NMOS and PMOS are divided into each other by isolation insulator layer 12a.

[0043] That is, NMOS is n+ formed in the epitaxial single-crystal-silicon layer 12. Source layer 13a and drain layer 13b of a mold, The channel field 14 formed among these, the gate electrode 16 formed through the gate insulating layer 15 on this, and p+ adjoined and formed in source layer 13a Contact layer 13c of a mold, It consists of source layer 13a, drain layer 13b and source electrode 17a that contacts contact layer 13c, respectively, drain electrode 17b, and contact electrode 17c. Source electrode 17a and contact electrode 17c are electrically connected to each other.

[0044] On the other hand, PMOS is n+ formed in the polish recon layer. It consists of source electrode 22a and drain electrode 22b which contact source layer 18a of a mold and drain layer 18b, the channel field 19 formed among these, the gate electrode 21 formed through the gate insulating layer 20 on this, source layer 18a, and drain layer 18b, respectively.

[0045] As mentioned above, in this operation gestalt, while forming the epitaxial single-crystal-silicon layer 12 on the silicon substrate in which IGBT was formed and forming NMOS in this crystal layer 12, PMOS is prepared on the polish recon layer formed on the oxide film 11.

Although a property with comparatively good PMOS formed in the polish recon layer is acquired, when NMOS is formed in a polish recon layer, compared with what was formed in single crystal silicon, channel mobility is low, and saturation characteristics are not acquired, either. However, according to this operation gestalt, good NMOS and good PMOS can be obtained in channel mobility and saturation characteristics, and increase of leakage current can be prevented.

[0046] Moreover, since NMOS is formed in the amorphous silicon layer 10 crystallized on p mold base layer 3, a threshold becomes proper. That is, although the surface concentration of p mold base layer of the usual IGBT may be too high for NMOS, if the amorphous silicon layer which is not doped is formed on p mold base layer, even if p mold impurity is spread in the crystallization amorphous silicon layer 10 from p mold base layer, the surface concentration of the p mold base layer concerned will become lower than that of p mold base layer of IGBT, and the threshold of NMOS will be rationalized.

[0047] It is p+ further again. p mold drain layer 1 of IGBT prepared in the silicon substrate since the mold diffusion layer 10 intervened between the silicon substrate and the epitaxial single-crystal-silicon layer 12, n mold base layer 2, p mold base layer 3, and n+ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by source layer 13a of a mold or drain layer 13b.

[0048] Thus, according to this operation gestalt, since good NMOS and a PMOS property can be acquired, it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with IGBT.

[0049] The manufacture approach of the high proof-pressure semiconductor device by this operation gestalt described above is as stating below. first, trench 1a of a vertical mold IGBT -- forming -- preceding -- the front face of p mold base layer 3 of a semi-conductor substrate -- p+ the mold diffusion layer 10 -- forming -- this p+ the field except the mold diffusion layer 10 and an IGBT formation schedule field -- alternative -- an oxide film 11 -- for example, LOCOS

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-- it forms by law. After forming an oxide film 11, this oxide-film 11 grade is used as a mask here, and it is p+ by an ion implantation etc. The mold diffusion layer 10 may be formed.

[0050] Next, p+ of p mold base layer 3 front face Apply on an oxide film 11 from the mold diffusion layer 10, and about 0.5 micrometers of amorphous silicon (a-Si) layers are made to deposit, at 600 degrees C, it anneals for about 20 hours and solid phase growth is carried out. It is p+ by this annealing. While single-crystal-izing the amorphous silicon layer on the mold diffusion layer 10 and becoming the epitaxial single-crystal-silicon layer 12, the amorphous silicon layer on an oxide film 11 turns into a polish recon layer.

[0051] Then, by the ion implantation, n mold impurity is introduced into the field to which PMOS of said polish recon layer is formed in the field in which NMOS of the epitaxial single-crystal-silicon layer 12 is formed in p mold impurity, respectively, and it considers as the p type semiconductor layer 14 and the n-type-semiconductor layer 19, respectively. Furthermore, isolation oxide-film 12a which divides these components into an oxidation part is formed by oxidizing the field except the field in which PMOS of the field in which NMOS of the epitaxial single-crystal-silicon layer 12 is formed, and said polish recon layer is formed.

[0052] Next, in order to form the gate of IGBT, trench 3a is formed in a silicon substrate. The gate oxide (15 20) of NMOS and PMOS is formed [the inside of trench 3a] in the front face of the epitaxial single-crystal-silicon layer 12 and the above-mentioned polish recon layer for gate oxide 6 at coincidence, respectively. Furthermore, the polish recon film is deposited so that a trench may be embedded on this, and the gate electrode 7 of IGBT is produced. This polish recon film is deposited also on the gate oxide (15 20) of NMOS and PMOS at coincidence, and can also form the gate electrode (16 21) of NMOS and PMOS.

[0053] next, the gate electrode 7 and a gate electrode (16 21) -- a mask -- carrying out -- respectively -- an ion implantation -- n+ of IGBT n+ of the mold source layer 4 and NMOS mold source layer 13a and the drain layer 13 -- p+ of b and PMOS Mold source layer 18a and drain layer 18b are formed. Moreover, p+ of IGBT p+ of the mold contact layer 5 and NMOS Mold contact layer 13c is formed by the ion implantation.

[0054] Then, n+ of IGBT The mold source layer 4 and p+ The drain electrode 9 is formed in the source electrode 8 and p mold drain layer 1 at the mold contact layer 5. To source layer 13a of NMOS, drain layer 13b, and contact layer 13c, respectively Source electrode 17a, Drain electrode 17b and contact electrode 17c are formed, source electrode 22a and drain electrode 22b are formed in source layer 18a of PMOS, and drain layer 18b, respectively, and the high proof-pressure semiconductor device of this operation gestalt is completed.

[0055] (2nd operation gestalt) Drawing 2 is the sectional view showing the high proof-pressure semiconductor device concerning the 2nd operation gestalt of this invention. The same sign is attached and shown in the same part as drawing 1 , and detailed explanation is omitted. The point that this operation gestalt differs from the 1st operation gestalt is a point that a part of epitaxial single-crystal-silicon layer is formed on an insulating-layer pattern, and the drain layer of NMOS and a part of channel field are formed in a part of this single-crystal-silicon layer.

[0056] As shown in drawing 2 , the trench gate mold vertical mold IGBT is formed in the semiconductor substrate as a high proof-pressure semiconductor device, and the CMOS mold semiconductor device described below is formed on the same chip as this high proof-pressure semiconductor device.

[0057] That is, on a silicon substrate, the insulating-layer pattern 11 is formed alternatively, and on this insulating-layer pattern 11, as it runs aground in part, the epitaxial single-crystal-silicon layer 12 is formed on p mold base layer 3. Moreover, the polycrystal (Pori) silicon layer is prepared on the insulating-layer pattern 11. NMOS is formed in the epitaxial single-crystal-silicon layer 12, PMOS is formed in the polish recon layer on the insulating-layer pattern 11, respectively, and NMOS and PMOS are divided into each other by isolation insulator layer 12b.

[0058] That is, NMOS is n+ formed in the epitaxial single-crystal-silicon layer 12. Source layer 31a and drain layer 31b of a mold, The channel field 32 formed among these, the gate electrode 34 formed through the gate insulating layer 33 on this, and p+ adjoined and formed in source layer 31a Contact layer 31c of a mold, It consists of drain electrode 35b in contact with source electrode 35a in contact with source layer 31a and contact layer 31c, and drain layer 31b. A part

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of drain layer 31b of NMOS and channel field 32 are formed in a part of epitaxial single-crystal-silicon layer 12 on the insulating-layer pattern 11, and source layer 31a is formed in a part of epitaxial single-crystal-silicon layer 12 of p mold base layer 3 front face where the insulating-layer pattern 11 does not exist.

[0059] On the other hand, PMOS is n⁺ formed in the polish recon layer. It consists of source electrode 45a and drain electrode 45b which contact source layer 41a of a mold and drain layer 41b, the channel field 42 formed among these, the gate electrode 44 formed through the gate insulating layer 43 on this, source layer 41a, and drain layer 41b, respectively.

[0060] According to this operation gestalt, in channel mobility and saturation characteristics, good NMOS and good PMOS can be obtained like the 1st operation gestalt, and increase of leakage current can be prevented. Moreover, it is also possible to rationalize the threshold of NMOS.

[0061] Also in this operation gestalt, like the 1st operation gestalt, it applies on the insulating-layer pattern 11 from p mold base layer 3 of a silicon substrate, and an amorphous silicon layer is formed, and this amorphous silicon layer is single-crystal-ized, using a silicon substrate as seed crystal. By this single crystal-ization, a part of part near seed crystal also single-crystal-izes the amorphous silicon layer on the insulating-layer pattern 11. By forming a part of channel field 32 of NMOS, and drain layer 31b in the part of this single-crystal-ized amorphous silicon layer, it is possible to prevent increase of the leakage current of NMOS certainly. Since especially the channel field 52 is close to the silicon substrate used as seed crystal, it is possible to acquire the crystallinity which may be set to the channel field 52, and the effectiveness of leakage current prevention is large. Furthermore, it is also possible to form in the polish recon field to which that point did not single-crystal-ize drain layer 31b for the channel field 32 of NMOS to the single crystal-ized field of an amorphous silicon layer, and increase of the leakage current of NMOS can be prevented also in this case.

[0062] p mold drain layer 1 of IGBT prepared in the silicon substrate further again since the insulating-layer pattern 11 intervened between the silicon substrate and the epitaxial single-crystal-silicon layer 12, n mold base layer 2, p mold base layer 3, and n⁺ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by drain layer 31b of a mold.

[0063] in addition, the 1st operation gestalt -- the same -- p⁺ of high concentration [front face / of p mold base layer 3 / layer / 3 / concerned / p mold base] a mold diffusion layer forms -- having -- this p⁺ The channel field 32, source layer 31a, and contact layer 31c may be made to be formed in the front face of a mold diffusion layer. p mold drain layer 1 of IGBT which this prepared in the silicon substrate like the 1st operation gestalt, n mold base layer 2, p mold base layer 3, and n⁺ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by source layer 31a of a mold.

[0064] Thus, according to this operation gestalt, since good NMOS and a PMOS property can be acquired, it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with IGBT.

[0065] (3rd operation gestalt) Drawing 3 is the sectional view showing the high proof-pressure semiconductor device concerning the 3rd operation gestalt of this invention. The same sign is attached and shown in the same part as drawing 2 , and detailed explanation is omitted. The point that this operation gestalt differs from the 2nd operation gestalt is a point that the drain layer of NMOS, all of channel fields, and a part of source layer are formed in a part of epitaxial single-crystal-silicon layer formed on the insulating-layer pattern.

[0066] As shown in drawing 3 , the trench gate mold vertical mold IGBT is formed in the semiconductor substrate as a high proof-pressure semiconductor device, and the CMOS mold semiconductor device described below is formed on the same chip as this high proof-pressure semiconductor device.

[0067] That is, on a silicon substrate, the insulating-layer pattern 11 is formed alternatively, and on this insulating-layer pattern 11, as it runs aground in part, the epitaxial single-crystal-silicon layer 12 is formed on p mold base layer 3. Moreover, on the insulating-layer pattern 11, 12f of polycrystal (Pori) silicon layers is prepared. NMOS is formed in the epitaxial single-crystal-silicon

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layer 12, PMOS (not shown) is formed in 12f of polish recon layers on the insulating-layer pattern 11, respectively, and NMOS and PMOS are divided into each other by isolation insulator layer 12c.

[0068] That is, NMOS is n⁺ formed in the epitaxial single-crystal-silicon layer 12. Source layer 51a and drain layer 51b of a mold, The channel field 52 formed among these, the gate electrode 54 formed through the gate insulating layer 53 on this, and p⁺ adjoined and formed in source layer 51a Contact layer 51c of a mold, It consists of drain electrode 55b in contact with source electrode 55a in contact with source layer 51a and contact layer 51c, and drain layer 51b. A part for drain layer 51b of NMOS and all of the channel fields 52 and a part of source layer 51a are formed in a part of epitaxial single-crystal-silicon layer 12 on the insulating-layer pattern 11, and a part of source layer 51a is formed in a part of epitaxial single-crystal-silicon layer 12 of p mold base layer 3 front face where the insulating-layer pattern 11 does not exist.

[0069] According to this operation gestalt, in channel mobility and saturation characteristics, good NMOS and good PMOS can be obtained like the 1st operation gestalt, and increase of leakage current can be prevented. Moreover, it is also possible to rationalize the threshold of NMOS.

[0070] Also in this operation gestalt, the amorphous silicon layer formed on the insulating-layer pattern 11 from p mold base layer 3 of a silicon substrate, having applied is single-crystal-ized like the 2nd operation gestalt, using a silicon substrate as seed crystal. When a part of part also with the amorphous silicon layer near seed crystal on the insulating-layer pattern 11 single-crystal-izes and forms a part for drain layer 51b of NMOS, and all of the channel fields 52, and a part of source layer 51a in the part of this single-crystal-ized amorphous silicon layer by this single crystal-ization, it is possible to prevent increase of the leakage current of NMOS certainly. Since especially the channel field 52 is close to the silicon substrate used as seed crystal, it is possible to acquire the crystallinity which may be set to the channel field 52, and the effectiveness of leakage current prevention is large. Furthermore, it is also possible to form in the polish recon field to which that point did not single-crystal-ize drain layer 51b for the channel field 52 of NMOS to the single crystal-ized field of an amorphous silicon layer, and increase of the leakage current of NMOS can be prevented also in this case. Moreover, since the channel field 52 of NMOS is completely insulated from the silicon substrate with this structure, as for this channel field 52, it is hard to be influenced of the potential of a silicon substrate, and a setup of a threshold and control become easy.

[0071] p mold drain layer 1 of IGBT prepared in the silicon substrate with the insulating-layer pattern 11 further again, n mold base layer 2, p mold base layer 3, and n⁺ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by drain layer 51b of a mold.

[0072] in addition, the 1st operation gestalt — the same — p⁺ of high concentration [front face / of p mold base layer 3 / layer / 3 / concerned / p mold base] a mold diffusion layer forms — having — this p⁺ Source layer 51a and contact layer 51c may be made to be formed in the front face of a mold diffusion layer. p mold drain layer 1 of IGBT which this prepared in the silicon substrate like the 1st operation gestalt, n mold base layer 2, p mold base layer 3, and n⁺ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by source layer 51a of a mold.

[0073] Thus, according to this operation gestalt, since good NMOS and a PMOS property can be acquired, it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with IGBT.

[0074] (4th operation gestalt) Drawing 4 is the sectional view showing the high proof-pressure semiconductor device concerning the 4th operation gestalt of this invention. The same sign is attached and shown in the same part as drawing 1 , and detailed explanation is omitted. The point that this operation gestalt differs from the 1st operation gestalt is a point that NMOS is formed in p mold base layer of IGBT of a silicon substrate, and high-concentration p type layer is formed between this NMOS and p mold base layer.

[0075] As shown in drawing 4 , the trench gate mold vertical mold IGBT is formed in the semiconductor substrate as a high proof-pressure semiconductor device, and the CMOS mold

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semiconductor device described below is formed on the same chip as this high proof-pressure semiconductor device.

[0076] That is, on a silicon substrate, the insulating-layer pattern 11 is formed alternatively, and 12g of polycrystal (Pori) silicon layers is prepared on this insulating-layer pattern 11. PMOS is formed in 12g of this polish recon layer. Moreover, rather than p mold base layer 3, low-concentration p type semiconductor layer 3b is formed alternatively, and NMOS is formed in the field in which NMOS in p mold base layer 3 is formed at this p type semiconductor layer 3b. NMOS and PMOS are divided into each other by 12d of isolation insulator layers.

[0077] That is, NMOS is n⁺ formed in p type semiconductor layer 3b. Source layer 61a and drain layer 61b of a mold, The channel field 62 formed among these, the gate electrode 64 formed through the gate insulating layer 63 on this, and p⁺ adjoined and formed in source layer 61a Contact layer 61c of a mold, It consists of drain electrode 65b in contact with source electrode 65a in contact with source layer 61a and contact layer 61c, and drain layer 61b. p⁺ of high concentration [b / under Above NMOS / p type semiconductor layer 3/ layer / 3 / p type semiconductor layer 3b / concerned / or / p mold base] Mold diffusion layer 3c is formed.

[0078] On the other hand, PMOS is n⁺ formed in 12g of polish recon layers. It consists of source electrode 75a and drain electrode 75b which contact source layer 71a of a mold and drain layer 71b, the channel field 72 formed among these, the gate electrode 74 formed through the gate insulating layer 73 on this, source layer 71a, and drain layer 71b, respectively.

[0079] According to this operation gestalt, since NMOS is formed in p type semiconductor layer 3b of a silicon substrate, NMOS will be formed in the crystalline good single crystal part, good NMOS and good PMOS can be obtained in channel mobility and saturation characteristics like the 1st operation gestalt, and increase of leakage current can be prevented.

[0080] Moreover, since NMOS is formed in the low-concentration p type semiconductor layer 3 rather than p mold base layer 3 of IGBT, it is also possible to rationalize the threshold of the NMOS concerned. Formation of this p type semiconductor layer 3 is performed in advance of formation of p mold base layer of IGBT.

[0081] p⁺ of high concentration [layer / 3 / p type semiconductor layer 3b or / p mold base] further again p mold drain layer 1 of IGBT prepared in the silicon substrate by mold diffusion layer 3c, n mold base layer 2, p mold base layer 3, and n⁺ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by source layer 61a of a mold or drain layer 61b.

[0082] Thus, according to this operation gestalt, since good NMOS and a PMOS property can be acquired, it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with IGBT.

[0083] (5th operation gestalt) Drawing 5 is the sectional view showing the high proof-pressure semiconductor device concerning the 5th operation gestalt of this invention. The same sign is attached and shown in the same part as drawing 4 , and detailed explanation is omitted. The point that this operation gestalt differs from the 4th operation gestalt is a point that diode is formed in the polycrystal (Pori) silicon layer formed on the insulating-layer pattern.

[0084] As shown in drawing 5 , the trench gate mold vertical mold IGBT is formed in the semiconductor substrate as a high proof-pressure semiconductor device, and the diode described below is formed on the same chip as this high proof-pressure semiconductor device.

[0085] That is, on a silicon substrate, the insulating-layer pattern 11 is formed alternatively, and the polycrystal (Pori) silicon layer is prepared on this insulating-layer pattern 11. Diode is formed in this polish recon layer. Moreover, rather than p mold base layer 3, low-concentration p type semiconductor layer 3b is formed alternatively, and NMOS is formed in the field in which NMOS in p mold base layer 3 is formed at this p type semiconductor layer 3b. NMOS and diode are divided into each other by isolation insulator layer 12e.

[0086] That is, NMOS is n⁺ formed in p type semiconductor layer 3b. Source layer 81a and drain layer 81b of a mold, The channel field 82 formed among these, the gate electrode 84 formed through the gate insulating layer 83 on this, and p⁺ adjoined and formed in source layer 81a Contact layer 81c of a mold, It consists of drain electrode 85b in contact with source electrode 85a in contact with source layer 81a and contact layer 81c, and drain layer 81b. p⁺ of high

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concentration [b / under Above NMOS / p type semiconductor layer 3/ layer / 3 / p type semiconductor layer 3b / concerned / or / p mold base] Mold diffusion layer 3c is formed.

[0087] On the other hand, diode is p+ formed in the polish recon layer. Anode layer 91a of a mold, and n+ It consists of anode electrode 92a and cathode electrode 92b which contact cathode layer 91b of a mold, anode layer 91a, and cathode layer 91b, respectively.

[0088] According to this operation gestalt, in channel mobility and saturation characteristics, good NMOS can be obtained like the 4th operation gestalt, and increase of leakage current can be prevented.

[0089] Moreover, it is also possible to rationalize the threshold of NMOS by the p type semiconductor layer 3 like the 4th operation gestalt. Furthermore, p+ p mold drain layer 1 of IGBT prepared in the silicon substrate by mold diffusion layer 3c, n mold base layer 2, p mold base layer 3, and n+ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by source layer 81a of a mold or drain layer 81b.

[0090] Thus, according to this operation gestalt, since a good NMOS property can be acquired, it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with IGBT.

[0091] In addition, this invention is not limited to the above-mentioned operation gestalt. For example, p+ Between the mold drain layer 1 and n mold base layer 2, high-concentration n mold buffer layer can be formed rather than the n mold base layer 2 concerned, and it is possible to raise conductivity.

[0092] Moreover, although the above-mentioned operation gestalt explained the high proof-pressure semiconductor device of a vertical mold, this invention is applicable also to the high proof-pressure semiconductor device of a horizontal type. In this case, a drain layer is formed in the semi-conductor substrate front face of the same side as a source layer.

[0093] At the above-mentioned operation gestalt, it is p+ further again. It is a drain layer, although IGBT which has the drain layer of a mold was mentioned as the example and explained n+ It is also possible to consider as a mold and to apply to various quantity proof-pressure semiconductor devices, such as an MOS mold quantity proof-pressure semiconductor device and other thyristors. In addition, it is possible to deform variously and to carry out in the range which does not deviate from the meaning of this invention.

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1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The sectional view showing the high proof-pressure semiconductor device concerning the 1st operation gestalt of this invention.

[Drawing 2] The sectional view showing the high proof-pressure semiconductor device concerning the 2nd operation gestalt of this invention.

[Drawing 3] The sectional view showing the high proof-pressure semiconductor device concerning the 3rd operation gestalt of this invention.

[Drawing 4] The sectional view showing the high proof-pressure semiconductor device concerning the 4th operation gestalt of this invention.

[Drawing 5] The sectional view showing the high proof-pressure semiconductor device concerning the 5th operation gestalt of this invention.

[Drawing 6] The sectional view showing the conventional high proof-pressure semiconductor device.

[Drawing 7] The property Fig. having shown the relation between the electrical potential difference of NMOS and PMOS, and a current.

[Description of Notations]

1 P+ Mold Drain Layer

2 N Mold Base Layer

3 P Mold Base Layer

3a Trench

4 N+ Mold Source Layer

5 P+ Mold Contact Layer

6 Gate Dielectric Film

7 Gate Electrode

8 Source Electrode

9 Drain Electrode

10 P+ Mold Diffusion Layer

11 Insulating-Layer Pattern

12 Epitaxial Single-Crystal-Silicon Layer

12a Isolation insulator layer

13a n+ Source layer of a mold

13b n+ Drain layer of a mold

13c Contact layer

14 Channel Field

15 Gate Insulating Layer

16 Gate Electrode

17a Source electrode

17b Drain electrode

17c Contact electrode

18a n+ Source layer of a mold

18b Drain layer

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19 Channel Field
20 Gate Insulating Layer
21 Gate Electrode
22a Source electrode
22b Drain electrode

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(19) 日本国特許庁 (J P)

(12) 公開特許公報 (A)

(11) 特許出願公開番号

特開2000-150664

(P2000-150664A)

(43) 公開日 平成12年5月30日 (2000.5.30)

(51) Int.Cl. ⁷	識別記号	F I	テーマコード [*] (参考)
H 0 1 L	21/8234	H 0 1 L 27/08	1 0 2 A 5 F 0 3 8
	27/088	27/04	H 5 F 0 4 0
	27/04	27/08	3 2 1 A 5 F 0 4 8
	21/822	29/78	3 0 1 J 5 F 1 1 0
	21/8238		3 0 1 K
審査請求 未請求 請求項の数19 O L (全 13 頁) 最終頁に続く			

(21) 出願番号 特願平10-324609

(22) 出願日 平成10年11月16日 (1998.11.16)

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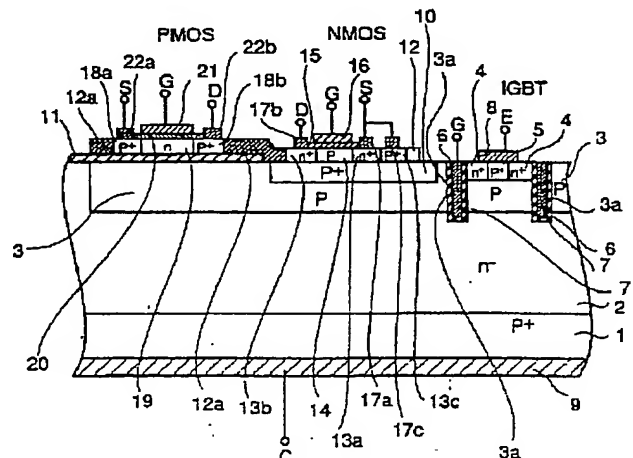
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(54) 【発明の名称】 高耐圧半導体装置

(57) 【要約】

【課題】 高耐圧素子及びドライブ回路や保護回路等を一体化した高耐圧半導体装置を信頼性高く低コストで提供すること。

【解決手段】 半導体基板表面に積層されたエピタキシャル単結晶半導体層10に形成されたソース層13a、ドレイン層13bと、ゲート絶縁膜15と、ゲート電極16とを有するn型のMOS型半導体素子と、前記半導体基板上に絶縁膜11を介して積層された多結晶半導体層に形成されたソース層18a、ドレイン層18bと、ゲート絶縁膜20と、ゲート電極21とを有するp型の第2のMOS型半導体素子と、前記半導体基板に形成されたIGBT等の高耐圧半導体素子とを具備する。



【特許請求の範囲】

【請求項 1】 半導体基板表面に形成された第 1 のソース層及び第 1 のドレイン層と、当該第 1 のソース層と第 1 のドレイン層間の前記半導体基板表面に第 1 のゲート絶縁膜を介して形成された第 1 のゲート電極とを有する n 型の第 1 の MOS 型半導体素子と、前記半導体基板上に絶縁膜を介して積層された多結晶半導体層に形成された第 2 のソース層及び第 2 のドレイン層と、当該第 2 のソース層と第 2 のドレイン層間の前記多結晶半導体層表面に第 2 のゲート絶縁膜を介して形成された第 2 のゲート電極とを有する p 型の第 2 の MOS 型半導体素子と、前記半導体基板に形成された高耐圧半導体素子とを具備することを特徴とする高耐圧半導体装置。

【請求項 2】 前記高耐圧半導体素子は、前記半導体基板に形成された n 型のベース層と、この n 型のベース層の表面に形成された p 型のベース層と、この p 型のベース層の表面に形成された n 型の第 3 のソース層及び p 型のコンタクト層と、前記 p 型のベース層の表面に第 3 のゲート絶縁膜を介して形成された第 3 のゲート電極と、前記 n 型のベース層の表面のうち前記 p 型のベース層から離れた位置に形成された第 3 のドレイン層と、前記第 3 のソース層及び前記 p 型のコンタクト層に接する第 1 のコンタクト電極と、前記第 3 のドレイン層に接する第 2 のコンタクト電極とを備えることを特徴とする請求項 1 記載の高耐圧半導体装置。

【請求項 3】 前記第 1 のソース層及び第 1 のドレイン層は、前記 p 型のベース層の表面に形成されていることを特徴とする請求項 2 記載の高耐圧半導体装置。

【請求項 4】 前記第 1 のソース層及び第 1 のドレイン層と前記 p 型のベース層との間には、当該 p 型のベース層よりも高濃度の p 型の半導体層が形成されていることを特徴とする請求項 3 記載の高耐圧半導体装置。

【請求項 5】 半導体基板表面に積層されたエピタキシャル単結晶半導体層に形成された第 1 のソース層及び第 1 のドレイン層と、当該第 1 のソース層と第 1 のドレイン層間の前記半導体基板表面に第 1 のゲート絶縁膜を介して形成された第 1 のゲート電極とを有する n 型の第 1 の MOS 型半導体素子と、前記半導体基板上に絶縁膜を介して積層された多結晶半導体層に形成された第 2 のソース層及び第 2 のドレイン層と、当該第 2 のソース層と第 2 のドレイン層間の前記多結晶半導体層表面に第 2 のゲート絶縁膜を介して形成された第 2 のゲート電極とを有する p 型の第 2 の MOS 型半導体素子と、前記半導体基板に形成された高耐圧半導体素子とを具備することを特徴とする高耐圧半導体装置。

【請求項 6】 前記高耐圧半導体素子は、前記半導体基板に形成された n 型のベース層と、この n 型のベース層の表面に形成された p 型のベース層と、この p 型のベース層の表面に形成された n 型の第 3 のソース層及び p 型のコンタクト層と、前記 p 型のベース層の表面に第 3 の

ゲート絶縁膜を介して形成された第 3 のゲート電極と、前記 n 型のベース層の表面のうち前記 p 型のベース層から離れた位置に形成された第 3 のドレイン層と、前記第 3 のソース層及び前記 p 型のコンタクト層に接する第 1 のコンタクト電極と、前記第 3 のドレイン層に接する第 2 のコンタクト電極とを備えることを特徴とする請求項 5 記載の高耐圧半導体装置。

【請求項 7】 前記エピタキシャル単結晶半導体層は、前記 p 型のベース層の表面に形成されていることを特徴とする請求項 6 記載の高耐圧半導体装置。

【請求項 8】 前記第 1 のソース層及び第 1 のドレイン層と前記 p 型のベース層との間には、当該 p 型のベース層よりも高濃度の p 型の半導体層が形成されていることを特徴とする請求項 7 記載の高耐圧半導体装置。

【請求項 9】 半導体基板上に絶縁膜が形成され、前記半導体基板表面から前記絶縁膜上にわたってエピタキシャル成長した半導体層に形成された第 1 のソース層及び第 1 のドレイン層と、当該第 1 のソース層と第 1 のドレイン層間の前記半導体層表面に第 1 のゲート絶縁膜を介して形成された第 1 のゲート電極とを有する n 型の第 1 の MOS 型半導体素子と、前記半導体層の前記絶縁膜上の部分に形成された第 2 のソース層及び第 2 のドレイン層と、この第 2 のソース層と第 2 のドレイン層間の前記半導体層表面に第 2 のゲート絶縁膜を介して形成された第 2 のゲート電極とを有する p 型の第 2 の MOS 型半導体素子と、前記半導体基板に形成された高耐圧半導体素子とを具備することを特徴とする高耐圧半導体装置。

【請求項 10】 前記第 1 の MOS 型半導体素子の第 1 のソース層は前記エピタキシャル成長した半導体層の前記半導体基板表面の部分に、当該素子の第 1 のドレイン層は前記半導体層の前記絶縁膜上の部分に、それぞれ形成されていることを特徴とする請求項 9 記載の高耐圧半導体装置。

【請求項 11】 前記高耐圧半導体素子は、前記半導体基板に形成された n 型のベース層と、この n 型のベース層の表面に形成された p 型のベース層と、この p 型のベース層の表面に形成された n 型の第 3 のソース層及び p 型のコンタクト層と、前記 p 型のベース層の表面に第 3 のゲート絶縁膜を介して形成された第 3 のゲート電極と、前記 n 型のベース層の表面のうち前記 p 型のベース層から離れた位置に形成された第 3 のドレイン層と、前記第 3 のソース層及び前記 p 型のコンタクト層に接する第 1 のコンタクト電極と、前記第 3 のドレイン層に接する第 2 のコンタクト電極とを備えることを特徴とする請求項 9 又は 10 記載の高耐圧半導体装置。

【請求項 12】 前記エピタキシャル成長した半導体層の前記第 1 のソース層が形成された部分は、前記 p 型のベース層の表面に形成されていることを特徴とする請求項 11 記載の高耐圧半導体装置。

【請求項 13】 前記第 1 のソース層と前記 p 型のベー

ス層との間には、当該 p 型のベース層よりも高濃度の p 型の半導体層が形成されていることを特徴とする請求項 12 記載の高耐圧半導体装置。

【請求項 14】 前記エピタキシャル成長した半導体層は単結晶からなり、前記半導体層の前記絶縁膜上の部分は多結晶からなることを特徴とする請求項 9 乃至 13 記載の高耐圧半導体装置。

【請求項 15】 前記第 3 のドレイン層は p 型層であることを特徴とする請求項 2 乃至 4、6 乃至 8、又は 11 乃至 14 記載の高耐圧半導体装置。

【請求項 16】 前記高耐圧半導体素子は縦型の半導体素子であり、前記第 3 のドレイン層は前記第 3 のソース層に対して反対側の前記 n 型のベース層の表面に形成されていることを特徴とする請求項 2 乃至 4、6 乃至 8、11 乃至 15 記載の高耐圧半導体装置。

【請求項 17】 前記第 3 のソース層及び前記 p 型のベース層を貫き前記 n 型のベース層に達するように溝が形成され、この溝の中に前記第 3 のゲート絶縁膜を介して前記第 3 のゲート電極が埋め込まれていることを特徴とする請求項 2 乃至 4、6 乃至 8、11 乃至 16 記載の高耐圧半導体装置。

【請求項 18】 前記 n 型のベース層と前記第 3 のドレイン層との間には、当該 n 型のベース層よりも高濃度の n 型の半導体層が形成されていることを特徴とする請求項 2 乃至 4、6 乃至 8、11 乃至 17 記載の高耐圧半導体装置。

【請求項 19】 前記 n 型の第 1 の MOS 型半導体素子と前記 p 型の第 2 の MOS 型半導体素子とは CMOS 回路を構成することを特徴とする請求項 1 乃至 18 記載の高耐圧半導体装置。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、高耐圧半導体装置に係わり、特に MOS 型半導体素子を有する高耐圧縦型半導体装置に関する。

【0002】

【従来の技術】IGBT (Insulated Gate Bipolar Transistor) 等の高耐圧素子はモータ制御、電源など多くの産業分野で使用されている。かかる高耐圧素子は大電力を扱うために、シリコン基板の表面と裏面をカソード、アノードまたはエミッタ、コレクタとする縦型素子が多く使われている。

【0003】このような IGBT 等の高耐圧素子、特に縦型素子を使い易くするためにドライブ回路や保護回路を一体化させ、高耐圧素子を壊れにくく、かつ高性能化することが行われている。通常このような回路は IGBT 等の高耐圧素子のチップとは別に作られ、同一パッケージに搭載するというモジュールの形態が採られる。

【0004】同一チップ上にこれらの回路を搭載できればコストと信頼性の面で飛躍的に有利になるが、従来技

術ではこれを容易に達成する手段がなかった。例えば、同一チップ上にドライブ回路や保護回路、例えば CMOS 回路等を作った場合には、IGBT 内部にキャリアプラズマが存在するため、n 型 MOS トランジスタ（以下、NMOS と略称する。）、p 型 MOS トランジスタ（以下、PMOS と略称する。）が簡単にラッチアップしてしまうという問題がある。

【0005】また、上記問題を解決するため、半導体基板に設けた IGBT 上に絶縁膜を介してポリシリコン層を形成し、このポリシリコン層に CMOS 回路を設けた高耐圧半導体装置がある。図 6 は、この高耐圧半導体装置の構造を示す断面図である。

【0006】図 6 に示すように、この高耐圧半導体装置はトレンチゲート型縦型高耐圧半導体装置である。半導体基板には高抵抗の n 型ベース層 2 が形成されており、この n 型ベース層 2 の一面には高濃度の p 型ドレイン層 1 が形成されている。p 型ドレイン層 1 にはドレイン電極 9 がコンタクトしている。また、n 型ベース層 2 の他方の面には p 型ベース層 3 が形成されており、この p 型ベース層 3 の表面には高濃度の n 型ソース層 4 及び高濃度の p 型コンタクト層 5 が形成されている。

【0007】さらに、上記半導体基板表面には複数のトレンチ 3a が形成されている。これらのトレンチ 3a はストライプ状の上面形状で互いに平行に配列されており（図示せず。）、n 型ソース層 4 及び p 型ベース層 3 を貫通して n 型ベース層 2 に到達するように形成されている。複数のトレンチ 3a の中にはゲート絶縁膜 6 を介してゲート電極 7 が埋め込まれている。

【0008】図 6 でも明らかなように、複数のトレンチ 3a 間の半導体基板表面の領域には上記 n 型ソース層 4 がゲート絶縁膜 6 と接して形成されており、n 型ソース層 4 に囲まれるようにして p 型コンタクト層 5 が形成されている。また、n 型ソース層 4 及び p 型コンタクト層 5 に接してソース電極 8 がコンタクトしている。

【0009】以上のように、高耐圧半導体素子としてトレンチゲート型縦型 IGBT が半導体基板に形成されており、この高耐圧半導体素子と同一チップ上に以下に述べる CMOS 型半導体素子が形成されている。

【0010】即ち、p 型ベース層 3 上には絶縁膜 121 を介して多結晶（ポリ）シリコン層 122 が形成され、このポリシリコン層 122 には NMOS 及び PMOS が形成されており、さらに NMOS と PMOS とは素子分離絶縁膜 122a によりお互いに分離されている。

【0011】NMOS は、ポリシリコン層 122 に形成されたソース層 101a 及びドレイン層 101b、これらの間に形成されたチャネル領域 102、この上にゲート絶縁層 103 を介して形成されたゲート電極 104、ソース層 101a 及びドレイン層 101b にそれぞれコンタクトするソース電極 105a 及びドレイン電極 105b から構成されている。

【0012】一方、PMOSは、ポリシリコン層122に形成されたソース層111a及びドレイン層111b、これらの間に形成されたチャネル領域112、この上にゲート絶縁層113を介して形成されたゲート電極114、ソース層111a及びドレイン層111bにそれぞれコンタクトするソース電極115a及びドレイン電極115bから構成されている。

【0013】以上のようにして同一チップ上にIGBT及びCMOS回路を一応搭載することはできる。しかしながら、半導体基板上に設けたポリシリコン層に形成したCMOS半導体素子は特性が悪く、高精度のアナログ回路を組むことができないという問題が生ずる。

【0014】即ち、ポリシリコン層に形成したPMOSは比較的良好な特性が得られるが、同じくポリシリコン層に形成したNMOSは単結晶シリコン層に形成したNMOSと比べてチャネル移動度が低く、飽和特性も得られない。図7は、ポリシリコン層に形成したNMOS及びPMOSのソース・ドレイン間電圧（横軸）とドレイン電流（縦軸）との関係を示す特性図である。図7

(a)はNMOSの場合の特性を示すもので、ソース・ドレイン間電圧の増加によりドレイン電流も増加し、飽和特性が得られないことがわかる。一方、図7(b)はPMOSの場合の特性を示すもので、ソース・ドレイン間電圧の増加によりドレイン電流も増加するが、飽和特性が得られることがわかる。

【0015】

【発明が解決しようとする課題】以上述べたように、高耐圧素子を使い易くするためにドライブ回路や保護回路を一体化させて、壊れにくく、かつ高性能化した高耐圧素子を信頼性高く低コストで提供することが試みられているが、従来技術ではこれを容易に達成する手段がなかった。

【0016】例えば、同一チップ上にドライブ回路や保護回路、例えばCMOS回路等を作った場合には、IGBT内部にキャリアプラズマが存在するため、NMOS及びPMOSが簡単にラッチアップしてしまうという問題がある。

【0017】また、半導体基板上に設けたポリシリコン層に形成したCMOS半導体素子は特性が悪く、高精度のアナログ回路を組むことができないという問題が生ずる。本発明は上記実情に鑑みてなされたものであり、高耐圧素子及びドライブ回路や保護回路等を一体化した高耐圧半導体装置を信頼性高く低コストで提供することを目的とするものである。

【0018】

【課題を解決するための手段】前述した課題を解決するために、本発明の第1は、半導体基板表面に形成された第1のソース層及び第1のドレイン層と、当該第1のソース層と第1のドレイン層間の前記半導体基板表面に第1のゲート絶縁膜を介して形成された第1のゲート電極

とを有するn型の第1のMOS型半導体素子と、前記半導体基板上に絶縁膜を介して積層された多結晶半導体層に形成された第2のソース層及び第2のドレイン層と、当該第2のソース層と第2のドレイン層間の前記多結晶半導体層表面に第2のゲート絶縁膜を介して形成された第2のゲート電極とを有するp型の第2のMOS型半導体素子と、前記半導体基板に形成された高耐圧半導体素子とを具備することを特徴とする高耐圧半導体装置を提供する。

【0019】また本発明の第2は、半導体基板表面に積層されたエピタキシャル単結晶半導体層に形成された第1のソース層及び第1のドレイン層と、当該第1のソース層と第1のドレイン層間の前記半導体基板表面に第1のゲート絶縁膜を介して形成された第1のゲート電極とを有するn型の第1のMOS型半導体素子と、前記半導体基板上に絶縁膜を介して積層された多結晶半導体層に形成された第2のソース層及び第2のドレイン層と、当該第2のソース層と第2のドレイン層間の前記多結晶半導体層表面に第2のゲート絶縁膜を介して形成された第2のゲート電極とを有するp型の第2のMOS型半導体素子と、前記半導体基板に形成された高耐圧半導体素子とを具備することを特徴とする高耐圧半導体装置を提供する。

【0020】また本発明の第3は、半導体基板上に絶縁膜が形成され、前記半導体基板表面から前記絶縁膜上にわたってエピタキシャル成長した半導体層に形成された第1のソース層及び第1のドレイン層と、当該第1のソース層と第1のドレイン層間の前記半導体層表面に第1のゲート絶縁膜を介して形成された第1のゲート電極とを有するn型の第1のMOS型半導体素子と、前記半導体層の前記絶縁膜上の部分に形成された第2のソース層及び第2のドレイン層と、この第2のソース層と第2のドレイン層間の前記半導体層表面に第2のゲート絶縁膜を介して形成された第2のゲート電極とを有するp型の第2のMOS型半導体素子と、前記半導体基板に形成された高耐圧半導体素子とを具備することを特徴とする高耐圧半導体装置を提供する。

【0021】上記した本発明において、以下の構成を具備することが好ましい。

(1) 本発明の第1、2、3において、前記高耐圧半導体素子は、前記半導体基板に形成されたn型のベース層と、このn型のベース層の表面に形成されたp型のベース層と、このp型のベース層の表面に形成されたn型の第3のソース層及びp型のコンタクト層と、前記p型のベース層の表面に第3のゲート絶縁膜を介して形成された第3のゲート電極と、前記n型のベース層の表面のうち前記p型のベース層から離れた位置に形成された第3のドレイン層と、前記第3のソース層及び前記p型のコンタクト層に接する第1のコンタクト電極と、前記第3のドレイン層に接する第2のコンタクト電極とを備える

こと。

【0022】(2) 本発明の第1、2、3において、前記第3のドレイン層はp型層であること。

(3) 本発明の第1、2、3において、前記高耐圧半導体素子は縦型の半導体素子であり、前記第3のドレイン層は前記第3のソース層に対して反対側の前記n型のベース層の表面に形成されていること。

【0023】(4) 本発明の第1、2、3において、前記第3のソース層及び前記p型のベース層を貫き前記n型のベース層に達するように溝が形成され、この溝の中に前記第3のゲート絶縁膜を介して前記第3のゲート電極が埋め込まれていること。

【0024】(5) 本発明の第1、2、3において、前記n型のベース層と前記第3のドレイン層との間には、当該n型のベース層よりも高濃度のn型の半導体層が形成されていること。

【0025】(6) 本発明の第1、2、3において、前記n型の第1のMOS型半導体素子と前記p型の第2のMOS型半導体素子とはCMOS回路を構成すること

(7) 本発明の第1において、前記第1のソース層及び第1のドレイン層は、前記p型のベース層の表面に形成されていること。

【0026】(8) 本発明の第2において、前記エピタキシャル単結晶半導体層は、前記p型のベース層の表面に形成されていること。

(9) 本発明の第1、2において、前記第1のソース層及び第1のドレイン層と前記p型のベース層との間には、当該p型のベース層よりも高濃度のp型の半導体層が形成されていること。

【0027】(10) 本発明の第3において、前記第1のMOS型半導体素子の第1のソース層は前記エピタキシャル成長した半導体層の前記半導体基板表面の部分に、当該素子の第1のドレイン層は前記半導体層の前記絶縁膜上の部分に、それぞれ形成されていること。

【0028】(11) 本発明の第3において、前記エピタキシャル成長した半導体層の前記第1のソース層が形成された部分は、前記p型のベース層の表面に形成されていること。

【0029】(12) 本発明の第3において、前記第1のソース層と前記p型のベース層との間には、当該p型のベース層よりも高濃度のp型の半導体層が形成されていること。

【0030】(13) 本発明の第3において、前記エピタキシャル成長した半導体層は単結晶からなり、前記半導体層の前記絶縁膜上の部分は多結晶からなること。本発明においては、例えば、IGBT等の高耐圧半導体素子と同じシリコン基板上又はこの上に設けたエピタキシャル結晶層にNMOSを形成し、PMOSは酸化膜上に設けたポリシリコン層上に設ける。

【0031】ポリシリコン層に形成したPMOSは比較

的良好な特性が得られるが、NMOSをポリシリコン層に形成した場合は単結晶シリコンに形成したものと比べてチャネル移動度が低く、飽和特性も得られない。本発明によれば、IGBT等はpベース拡散層を持つため、特に本発明の第1のように、このpベース拡散層中に比較的容易にNMOSを形成することができる。この構成によれば良好なNMOS特性を得ることが可能である。

【0032】かかる構成では、IGBT等の内部に存在するプラズマのためリーク電流が大きくなってしまふ場合があるので、以下に示す構成がより好ましい。即ち、NMOSのpベース電位がIGBT等の高耐圧半導体素子のソース電位と同じになるように、当該pベースとソースとの間にショート電極を設けておくことが望ましい。

【0033】また、本発明の第2及び第3においては、例えば、シリコン基板上にシリコン酸化膜パターンを設け、pベース上からこのシリコン酸化膜パターン上にかけてアモルファスシリコン層を設け、これを600℃程度でアニールして結晶化する方法を用いることが可能である。この方法により、上記pベース上にはエピタキシャル成長シリコン層が形成され、この層にNMOSを作製することができ、また上記シリコン酸化膜パターン上にはポリシリコン層が形成され、この層にPMOSを作製することができる。その結果、かかるポリシリコン層に形成したPMOS、及びエピタキシャル成長シリコン層に形成したNMOSともども、チャネル移動度及び飽和特性において良好な特性を得ることが可能となる。

【0034】さらにまた、上記したシリコン酸化膜パターン上に延在させたアモルファスシリコン層の一部は、上記pベースに近い部分において、単結晶のエピタキシャル成長層とすることも可能である。したがって、この部分にNMOSのドレイン、チャネル(ベース)、又はソースを形成することが可能である。例えば、NMOSのソースはpベース上のエピタキシャル成長層に、チャネル(ベース)はシリコン酸化膜パターン上の単結晶エピタキシャル成長層に、ドレインは当該酸化膜パターン上のエピタキシャル成長層(単結晶若しくはポリシリコン)に設ける。

【0035】かかる構成によれば、チャネル移動度及び飽和特性において良好な特性を得ることができ、リーク電流の増大を防止することができる。さらに、ドレインはシリコン酸化膜パターン上に存在するので、シリコン基板に設けたIGBTのp型ドレイン層、高抵抗n型層、p型ベース層、及びNMOSのn型ソース層によって寄生サイリスタが構成されることを防止でき、素子のサイリスタ動作を抑制することが可能である。

【0036】以上のように、本発明によれば、NMOSを半導体基板、若しくはその上のエピタキシャル成長層に設け、PMOSを絶縁膜上の多結晶層に設けるので、良好なNMOS及びPMOS特性を得ることができ、ド

ライブ回路や保護回路等のアナログ、デジタル各種回路を高精度で IGBT 等の高耐压半導体素子と一体的に構成することが可能である。

【0037】

【発明の実施の形態】以下、本発明の高耐压半導体装置に係る実施形態について図面を用いつつ詳細に説明する。

（第1の実施形態）図1は、本発明の第1の実施形態に係る高耐压半導体装置を示す断面図である。本実施形態の高耐压半導体装置はトレンチゲート型縦型 IGBT

である。
【0038】図1に示すように、半導体基板（シリコン基板）には高抵抗の n 型ベース層2が形成されており、この n 型ベース層2の一面には高濃度の p⁺ 型ドレイン層1が形成されている。p 型ドレイン層1にはドレイン電極9がコンタクトしている。また、n 型ベース層2の他方の面には p 型ベース層3が形成されており、この p 型ベース層3の表面には高濃度の n⁺ 型ソース層4及び高濃度の p⁺ 型コンタクト層5が形成されている。

【0039】さらに、上記半導体基板表面には複数のトレンチ3aが形成されている。これらのトレンチ3aはストライプ状の上面形状で互いに平行に配列されており（図示せず。）、n⁺ 型ソース層4及び p 型ベース層3を貫通して n 型ベース層2に到達するように形成されている。複数のトレンチ3aの中にはゲート絶縁膜6を介してゲート電極7が埋め込まれている。

【0040】図1でも明らかなように、複数のトレンチ3a間の半導体基板表面の領域には上記 n⁺ 型ソース層4がゲート絶縁膜6と接して形成されており、n⁺ 型ソース層4に囲まれるようにして p⁺ 型コンタクト層5が形成されている。また、n⁺ 型ソース層4及び p⁺ 型コンタクト層5に接してソース電極8がコンタクトしている。p⁺ 型コンタクト層5はトレンチ3a間に複数配置されていても良く、n⁺ 型ソース層4及び p⁺ 型コンタクト層5に対するソース電極8のコンタクトを確実に取るため、当該 n⁺ 型ソース層4及び p⁺ 型コンタクト層5はトレンチ1aの長手方向に沿って交互に配置されていることが望ましい。

【0041】以上のように、高耐压半導体素子としてトレンチゲート型縦型 IGBT が半導体基板に形成されており、この高耐压半導体素子と同一チップ上に以下に述べる CMOS 型半導体素子が形成されている。

【0042】即ち、p 型ベース層3の表面には当該 p 型ベース層3よりも高濃度の p⁺ 型拡散層10が形成され、この p⁺ 型拡散層10上にエピタキシャル単結晶シリコン層12が設けられている。一方、p⁺ 型拡散層10と異なる領域には絶縁層パターン11が形成され、この絶縁層パターン11上には多結晶（ポリ）シリコン層が設けられている。エピタキシャル単結晶シリコン層12には NMOS が、絶縁層パターン11上のポリシリコ

ン層には PMOS がそれぞれ形成されており、NMOS と PMOS とは素子分離絶縁膜12aによりお互いに分離されている。

【0043】即ち、NMOS は、エピタキシャル単結晶シリコン層12に形成された n⁺ 型のソース層13a及びドレイン層13b、これらの間に形成されたチャネル領域14、この上にゲート絶縁層15を介して形成されたゲート電極16、ソース層13aに隣接して形成された p⁺ 型のコンタクト層13c、ソース層13a、ドレイン層13b、及びコンタクト層13cにそれぞれコンタクトするソース電極17a、ドレイン電極17b、及びコンタクト電極17cから構成されている。ソース電極17aとコンタクト電極17cとはお互いに電氣的に接続されている。

【0044】一方、PMOS は、ポリシリコン層に形成された n⁺ 型のソース層18a及びドレイン層18b、これらの間に形成されたチャネル領域19、この上にゲート絶縁層20を介して形成されたゲート電極21、ソース層18a及びドレイン層18bにそれぞれコンタクトするソース電極22a及びドレイン電極22bから構成されている。

【0045】以上のように、本実施形態においては、IGBT が形成されたシリコン基板上にエピタキシャル単結晶シリコン層12を設け、この結晶層12に NMOS を形成するとともに、PMOS は酸化膜11上に形成されたポリシリコン層上に設ける。ポリシリコン層に形成した PMOS は比較的良好な特性が得られるが、NMOS をポリシリコン層に形成した場合は単結晶シリコンに形成したもの比べてチャネル移動度が低く、飽和特性も得られない。しかしながら、本実施形態によれば、チャネル移動度及び飽和特性において良好な NMOS 及び PMOS を得ることができ、リーク電流の増大を防止することができる。

【0046】また、NMOS は p 型ベース層3上の結晶化したアモルファスシリコン層10に形成されるので、閾値は適正になる。即ち、通常の IGBT の p 型ベース層の表面濃度は NMOS には高すぎる場合があるが、ドーピングされていないアモルファスシリコン層を p 型ベース層上に形成すると、p 型不純物が p 型ベース層から結晶化アモルファスシリコン層10に拡散しても、当該 p 型ベース層の表面濃度は IGBT の p 型ベース層のそれよりも低くなり、NMOS の閾値が適正化される。

【0047】さらにまた、p⁺ 型拡散層10がシリコン基板とエピタキシャル単結晶シリコン層12との間に介在するので、シリコン基板に設けた IGBT の p 型ドレイン層1、n 型ベース層2、p 型ベース層3、及び NMOS の n⁺ 型のソース層13a又はドレイン層13bによって寄生サイリスタが構成されることを防止でき、素子のサイリスタ動作を抑制することが可能である。

【0048】このように、本実施形態によれば、良好な

NMOS及びPMOS特性を得ることができるため、ドライブ回路や保護回路等のアナログ、デジタル各種回路を高精度でIGBTと一体的に構成することが可能である。

【0049】以上述べた本実施形態による高耐圧半導体装置の製造方法は、以下に述べる通りである。まず、縦型IGBTのトレンチ1aを形成するに先立ち、半導体基板のp型ベース層3の表面にp⁺型拡散層10を形成し、このp⁺型拡散層10及びIGBT形成予定領域を除く領域に選択的に酸化膜11を、例えばLOCOS法によって形成する。ここで、酸化膜11を形成した後、この酸化膜11等をマスクにしてイオン注入等によりp⁺型拡散層10を形成しても良い。

【0050】次に、p型ベース層3表面のp⁺型拡散層10から酸化膜11上にかけてアモルファスシリコン(a-Si)層を0.5μm程度堆積させ、600℃で20時間程度アニールして固相成長させる。このアニールによりp⁺型拡散層10上のアモルファスシリコン層は単結晶化してエピタキシャル単結晶シリコン層12となる一方、酸化膜11上のアモルファスシリコン層はポリシリコン層となる。

【0051】この後、イオン注入により、エピタキシャル単結晶シリコン層12のNMOSが形成される領域にはp型不純物を、前記ポリシリコン層のPMOSが形成される領域にはn型不純物をそれぞれ導入して、それぞれp型半導体層14及びn型半導体層19とする。さらに、エピタキシャル単結晶シリコン層12のNMOSが形成される領域及び前記ポリシリコン層のPMOSが形成される領域を除く領域を酸化することにより、酸化部分にこれらの素子を分離する素子分離酸化膜12aを形成する。

【0052】次に、IGBTのゲートを形成するためにトレンチ3aをシリコン基板に形成する。トレンチ3aの内面にはゲート酸化膜6を、エピタキシャル単結晶シリコン層12及び上記ポリシリコン層の表面にはNMOS及びPMOSのゲート酸化膜(15、20)をそれぞれ同時に形成する。さらに、この上にトレンチを埋め込むようにポリシリコン膜を堆積し、IGBTのゲート電極7を作製する。このポリシリコン膜は同時にNMOS及びPMOSのゲート酸化膜(15、20)上にも堆積して、NMOS及びPMOSのゲート電極(16、21)をも形成することができる。

【0053】次に、ゲート電極7、ゲート電極(16、21)をマスクとして、それぞれイオン注入によりIGBTのn⁺型ソース層4、NMOSのn⁺型ソース層13a及びドレイン層13b、PMOSのp⁺型ソース層18a及びドレイン層18bを形成する。また、IGBTのp⁺型コンタクト層5及びNMOSのp⁺型コンタクト層13cをイオン注入により形成する。

【0054】この後、IGBTのn⁺型ソース層4及び

p⁺型コンタクト層5にはソース電極8、p型ドレイン層1にはドレイン電極9を形成し、NMOSのソース層13a、ドレイン層13b、及びコンタクト層13cにはそれぞれソース電極17a、ドレイン電極17b、及びコンタクト電極17cを形成し、PMOSのソース層18a及びドレイン層18bにはそれぞれソース電極22a及びドレイン電極22bを形成して、本実施形態の高耐圧半導体装置が完成する。

【0055】(第2の実施形態)図2は、本発明の第2の実施形態に係わる高耐圧半導体装置を示す断面図である。図1と同一部分には同一の符号を付して示し詳細な説明は省略する。本実施形態が第1の実施形態と異なる点は、エピタキシャル単結晶シリコン層の一部分が絶縁層パターン上に形成され、この単結晶シリコン層の一部分にNMOSのドレイン層及びチャネル領域の一部が形成されている点である。

【0056】図2に示すように、高耐圧半導体素子としてトレンチゲート型縦型IGBTが半導体基板に形成されており、この高耐圧半導体素子と同一チップ上に以下に述べるCMOS型半導体素子が形成されている。

【0057】即ち、シリコン基板には選択的に絶縁層パターン11が形成され、この絶縁層パターン11上に一部乗り上げるようにしてp型ベース層3上にエピタキシャル単結晶シリコン層12が設けられている。また、絶縁層パターン11上には多結晶(ポリ)シリコン層が設けられている。エピタキシャル単結晶シリコン層12にはNMOSが、絶縁層パターン11上のポリシリコン層にはPMOSがそれぞれ形成されており、NMOSとPMOSとは素子分離絶縁膜12bによりお互いに分離されている。

【0058】即ち、NMOSは、エピタキシャル単結晶シリコン層12に形成されたn⁺型のソース層31a及びドレイン層31b、これらの間に形成されたチャネル領域32、この上にゲート絶縁層33を介して形成されたゲート電極34、ソース層31aに隣接して形成されたp⁺型のコンタクト層31c、ソース層31a及びコンタクト層31cにコンタクトするソース電極35a、ドレイン層31bにコンタクトするドレイン電極35bから構成されている。NMOSのドレイン層31b及びチャネル領域32の一部は絶縁層パターン11上のエピタキシャル単結晶シリコン層12の一部分に形成され、ソース層31aは絶縁層パターン11が存在しないp型ベース層3表面のエピタキシャル単結晶シリコン層12の一部分に形成されている。

【0059】一方、PMOSは、ポリシリコン層に形成されたn⁺型のソース層41a及びドレイン層41b、これらの間に形成されたチャネル領域42、この上にゲート絶縁層43を介して形成されたゲート電極44、ソース層41a及びドレイン層41bにそれぞれコンタクトするソース電極45a及びドレイン電極45bから構

成されている。

【0060】本実施形態によれば、第1の実施形態と同様にチャネル移動度及び飽和特性において良好なNMOS及びPMOSを得ることができ、リーク電流の増大を防止することができる。また、NMOSの閾値を適正化することも可能である。

【0061】本実施形態においても第1の実施形態と同様に、シリコン基板のp型ベース層3から絶縁層パターン11上にかけてアモルファスシリコン層を形成し、このアモルファスシリコン層をシリコン基板を種結晶として単結晶化する。この単結晶化によって、絶縁層パターン11上のアモルファスシリコン層も種結晶に近い部分が一部単結晶化する。この単結晶化したアモルファスシリコン層の部分にNMOSのチャネル領域32の一部及びドレイン層31bを形成することにより、NMOSのリーク電流の増大を確実に防止することが可能である。特に、チャネル領域52は種結晶となるシリコン基板に近いので、チャネル領域52において良い結晶性を得ることが可能であり、リーク電流防止の効果は大きい。さらに、NMOSのチャネル領域32をアモルファスシリコン層の単結晶化領域に、ドレイン層31bをその先の単結晶化しなかったポリシリコン領域に形成することも可能であり、この場合にもNMOSのリーク電流の増大を防止することができる。

【0062】さらにまた、絶縁層パターン11がシリコン基板とエピタキシャル単結晶シリコン層12との間に介在するので、シリコン基板に設けたIGBTのp型ドレイン層1、n型ベース層2、p型ベース層3、及びNMOSのn⁺型のドレイン層31bによって寄生サイリスタが構成されることを防止でき、素子のサイリスタ動作を抑制することが可能である。

【0063】なお、第1の実施形態と同様にp型ベース層3の表面には当該p型ベース層3よりも高濃度のp⁺型拡散層が形成され、このp⁺型拡散層の表面にチャネル領域32、ソース層31a、コンタクト層31cが形成されるようにしても良い。これにより、第1の実施形態と同様に、シリコン基板に設けたIGBTのp型ドレイン層1、n型ベース層2、p型ベース層3、及びNMOSのn⁺型のソース層31aによって寄生サイリスタが構成されることを防止でき、素子のサイリスタ動作を抑制することが可能である。

【0064】このように、本実施形態によれば、良好なNMOS及びPMOS特性を得ることができるため、ドライブ回路や保護回路等のアナログ、デジタル各種回路を高精度でIGBTと一体的に構成することが可能である。

【0065】（第3の実施形態）図3は、本発明の第3の実施形態に係わる高耐圧半導体装置を示す断面図である。図2と同一部分には同一の符号を付して示し詳細な説明は省略する。本実施形態が第2の実施形態と異なる

点は、絶縁層パターン上に形成されたエピタキシャル単結晶シリコン層の一部分に、NMOSのドレイン層、チャネル領域の全部、及びソース層の一部が形成されている点である。

【0066】図3に示すように、高耐圧半導体素子としてトレンチゲート型縦型IGBTが半導体基板に形成されており、この高耐圧半導体素子と同一チップ上に以下に述べるCMOS型半導体素子が形成されている。

【0067】即ち、シリコン基板には選択的に絶縁層パターン11が形成され、この絶縁層パターン11上に一部乗り上げるようにしてp型ベース層3上にエピタキシャル単結晶シリコン層12が設けられている。また、絶縁層パターン11上には多結晶（ポリ）シリコン層12fが設けられている。エピタキシャル単結晶シリコン層12にはNMOSが、絶縁層パターン11上のポリシリコン層12fにはPMOS（図示せず）がそれぞれ形成されており、NMOSとPMOSとは素子分離絶縁膜12cによりお互いに分離されている。

【0068】即ち、NMOSは、エピタキシャル単結晶シリコン層12に形成されたn⁺型のソース層51a及びドレイン層51b、これらの間に形成されたチャネル領域52、この上にゲート絶縁層53を介して形成されたゲート電極54、ソース層51aに隣接して形成されたp⁺型のコンタクト層51c、ソース層51a及びコンタクト層51cにコンタクトするソース電極55a、ドレイン層51bにコンタクトするドレイン電極55bから構成されている。NMOSのドレイン層51b、チャネル領域52の全部分、及びソース層51aの一部分は絶縁層パターン11上のエピタキシャル単結晶シリコン層12の一部分に形成され、ソース層51aの一部分は絶縁層パターン11が存在しないp型ベース層3表面のエピタキシャル単結晶シリコン層12の一部分に形成されている。

【0069】本実施形態によれば、第1の実施形態と同様にチャネル移動度及び飽和特性において良好なNMOS及びPMOSを得ることができ、リーク電流の増大を防止することができる。また、NMOSの閾値を適正化することも可能である。

【0070】本実施形態においても第2の実施形態と同様に、シリコン基板のp型ベース層3から絶縁層パターン11上にかけて形成したアモルファスシリコン層を、シリコン基板を種結晶として単結晶化する。この単結晶化によって、絶縁層パターン11上のアモルファスシリコン層も種結晶に近い部分が一部単結晶化し、この単結晶化したアモルファスシリコン層の部分にNMOSのドレイン層51b、チャネル領域52の全部分、及びソース層51aの一部分を形成することにより、NMOSのリーク電流の増大を確実に防止することが可能である。特に、チャネル領域52は種結晶となるシリコン基板に近いので、チャネル領域52において良い結晶性を得る

ことが可能であり、リーク電流防止の効果は大きい。さらに、NMOSのチャネル領域52をアモルファスシリコン層の単結晶化領域に、ドレイン層51bをその先の単結晶化しなかったポリシリコン領域に形成することも可能であり、この場合にもNMOSのリーク電流の増大を防止することができる。また、かかる構造ではNMOSのチャネル領域52がシリコン基板から完全に絶縁されているので、かかるチャネル領域52はシリコン基板の電位の影響を受け難く、しきい値の設定、制御が容易になる。

【0071】さらにまた、絶縁層パターン11により、シリコン基板に設けたIGBTのp型ドレイン層1、n型ベース層2、p型ベース層3、及びNMOSのn+型のドレイン層51bによって寄生サイリスタが構成されることを防止でき、素子のサイリスタ動作を抑制することが可能である。

【0072】なお、第1の実施形態と同様にp型ベース層3の表面には当該p型ベース層3よりも高濃度のp+型拡散層が形成され、このp+型拡散層の表面にソース層51a、コンタクト層51cが形成されるようにしても良い。これにより、第1の実施形態と同様に、シリコン基板に設けたIGBTのp型ドレイン層1、n型ベース層2、p型ベース層3、及びNMOSのn+型のソース層51aによって寄生サイリスタが構成されることを防止でき、素子のサイリスタ動作を抑制することが可能である。

【0073】このように、本実施形態によれば、良好なNMOS及びPMOS特性を得ることができるため、ドライブ回路や保護回路等のアナログ、デジタル各種回路を高精度でIGBTと一体的に構成することが可能である。

【0074】(第4の実施形態)図4は、本発明の第4の実施形態に係わる高耐圧半導体装置を示す断面図である。図1と同一部分には同一の符号を付して示し詳細な説明は省略する。本実施形態が第1の実施形態と異なる点は、シリコン基板のIGBTのp型ベース層にNMOSが形成され、このNMOSとp型ベース層との間に高濃度のp型層が形成されている点である。

【0075】図4に示すように、高耐圧半導体素子としてトレンチゲート型縦型IGBTが半導体基板に形成されており、この高耐圧半導体素子と同一チップ上に以下に述べるCMOS型半導体素子が形成されている。

【0076】即ち、シリコン基板上には選択的に絶縁層パターン11が形成され、この絶縁層パターン11上には多結晶(ポリ)シリコン層12gが設けられている。このポリシリコン層12gにはPMOSが形成されている。また、p型ベース層3中のNMOSが形成される領域には、p型ベース層3よりも低濃度のp型半導体層3bが選択的に形成され、このp型半導体層3bにNMOSが形成されている。NMOSとPMOSとは素子分離

絶縁膜12dによりお互いに分離されている。

【0077】即ち、NMOSは、p型半導体層3bに形成されたn+型のソース層61a及びドレイン層61b、これらの間に形成されたチャネル領域62、この上にゲート絶縁層63を介して形成されたゲート電極64、ソース層61aに隣接して形成されたp+型のコンタクト層61c、ソース層61a及びコンタクト層61cにコンタクトするソース電極65a、ドレイン層61bにコンタクトするドレイン電極65bから構成されている。上記NMOS下のp型半導体層3bには当該p型半導体層3b又はp型ベース層3よりも高濃度のp+型拡散層3cが形成されている。

【0078】一方、PMOSは、ポリシリコン層12gに形成されたn+型のソース層71a及びドレイン層71b、これらの間に形成されたチャネル領域72、この上にゲート絶縁層73を介して形成されたゲート電極74、ソース層71a及びドレイン層71bにそれぞれコンタクトするソース電極75a及びドレイン電極75bから構成されている。

【0079】本実施形態によれば、シリコン基板のp型半導体層3bにNMOSが形成されているので、結晶性の良い単結晶部分にNMOSが形成されていることになり、第1の実施形態と同様にチャネル移動度及び飽和特性において良好なNMOS及びPMOSを得ることができ、リーク電流の増大を防止することができる。

【0080】また、IGBTのp型ベース層3よりも低濃度のp型半導体層3にNMOSが形成されているので、当該NMOSの閾値を適正化することも可能である。このp型半導体層3の形成は、IGBTのp型ベース層の形成に先立って行われる。

【0081】さらにまた、p型半導体層3b又はp型ベース層3よりも高濃度のp+型拡散層3cにより、シリコン基板に設けたIGBTのp型ドレイン層1、n型ベース層2、p型ベース層3、及びNMOSのn+型のソース層61a又はドレイン層61bによって寄生サイリスタが構成されることを防止でき、素子のサイリスタ動作を抑制することが可能である。

【0082】このように、本実施形態によれば、良好なNMOS及びPMOS特性を得ることができるため、ドライブ回路や保護回路等のアナログ、デジタル各種回路を高精度でIGBTと一体的に構成することが可能である。

【0083】(第5の実施形態)図5は、本発明の第5の実施形態に係わる高耐圧半導体装置を示す断面図である。図4と同一部分には同一の符号を付して示し詳細な説明は省略する。本実施形態が第4の実施形態と異なる点は、絶縁層パターン上に形成された多結晶(ポリ)シリコン層にダイオードが形成されている点である。

【0084】図5に示すように、高耐圧半導体素子としてトレンチゲート型縦型IGBTが半導体基板に形成さ

れており、この高耐圧半導体素子と同一チップ上に以下に述べるダイオードが形成されている。

【0085】即ち、シリコン基板には選択的に絶縁層パターン11が形成され、この絶縁層パターン11上には多結晶（ポリ）シリコン層が設けられている。このポリシリコン層にはダイオードが形成されている。また、p型ベース層3中のNMOSが形成される領域には、p型ベース層3よりも低濃度のp型半導体層3bが選択的に形成され、このp型半導体層3bにNMOSが形成されている。NMOSとダイオードとは素子分離絶縁膜12eによりお互いに分離されている。

【0086】即ち、NMOSは、p型半導体層3bに形成されたn⁺型のソース層81a及びドレイン層81b、これらの間に形成されたチャネル領域82、この上にゲート絶縁層83を介して形成されたゲート電極84、ソース層81aに隣接して形成されたp⁺型のコンタクト層81c、ソース層81a及びコンタクト層81cにコンタクトするソース電極85a、ドレイン層81bにコンタクトするドレイン電極85bから構成されている。上記NMOS下のp型半導体層3bには当該p型半導体層3b又はp型ベース層3よりも高濃度のp⁺型拡散層3cが形成されている。

【0087】一方、ダイオードは、ポリシリコン層に形成されたp⁺型のアノード層91a、n⁺型のカソード層91b、アノード層91a及びカソード層91bにそれぞれコンタクトするアノード電極92a及びカソード電極92bから構成されている。

【0088】本実施形態によれば、第4の実施形態と同様にチャネル移動度及び飽和特性において良好なNMOSを得ることができ、リーク電流の増大を防止することができる。

【0089】また、第4の実施形態と同様にp型半導体層3によりNMOSの閾値を適正化することも可能である。さらに、p⁺型拡散層3cにより、シリコン基板に設けたIGBTのp型ドレイン層1、n型ベース層2、p型ベース層3、及びNMOSのn⁺型のソース層81a又はドレイン層81bによって寄生サイリスタが構成されることを防止でき、素子のサイリスタ動作を抑制することが可能である。

【0090】このように、本実施形態によれば、良好なNMOS特性を得ることができるため、ドライブ回路や保護回路等のアナログ、デジタル各種回路を高精度でIGBTと一体的に構成することが可能である。

【0091】なお、本発明は上記実施形態に限定されるものではない。例えば、p⁺型ドレイン層1とn型ベース層2との間には当該n型ベース層2よりも高濃度のn型バッファ層を形成することができ、導電率を向上させることが可能である。

【0092】また、上記実施形態では縦型の高耐圧半導体装置について説明したが、本発明は横型の高耐圧半導

体装置に対しても適用可能である。この場合、ドレイン層はソース層と同じ側の半導体基板表面に形成する。

【0093】さらにまた、上記実施形態ではp⁺型のドレイン層を有するIGBTを例に挙げて説明したが、ドレイン層をn⁺型としてMOS型高耐圧半導体素子、その他サイリスタ等、各種高耐圧半導体素子に対して適用することも可能である。その他、本発明の趣旨を逸脱しない範囲で種々変形して実施することが可能である。

【0094】

【発明の効果】本発明によれば、高耐圧素子及びドライブ回路や保護回路等を一体化した高耐圧半導体装置を信頼性高く低コストで提供することができる。

【図面の簡単な説明】

【図1】 本発明の第1の実施形態に係わる高耐圧半導体装置を示す断面図。

【図2】 本発明の第2の実施形態に係わる高耐圧半導体装置を示す断面図。

【図3】 本発明の第3の実施形態に係わる高耐圧半導体装置を示す断面図。

【図4】 本発明の第4の実施形態に係わる高耐圧半導体装置を示す断面図。

【図5】 本発明の第5の実施形態に係わる高耐圧半導体装置を示す断面図。

【図6】 従来の高耐圧半導体装置を示す断面図。

【図7】 NMOS及びPMOSの電圧と電流との関係を示した特性図。

【符号の説明】

1 p⁺型ドレイン層

2 n型ベース層

3 p型ベース層

3a トレンチ

4 n⁺型ソース層

5 p⁺型コンタクト層

6 ゲート絶縁膜

7 ゲート電極

8 ソース電極

9 ドレイン電極

10 p⁺型拡散層

11 絶縁層パターン

12 エピタキシャル単結晶シリコン層

12a 素子分離絶縁膜

13a n⁺型のソース層

13b n⁺型のドレイン層

13c コンタクト層

14 チャネル領域

15 ゲート絶縁層

16 ゲート電極

17a ソース電極

17b ドレイン電極

17c コンタクト電極

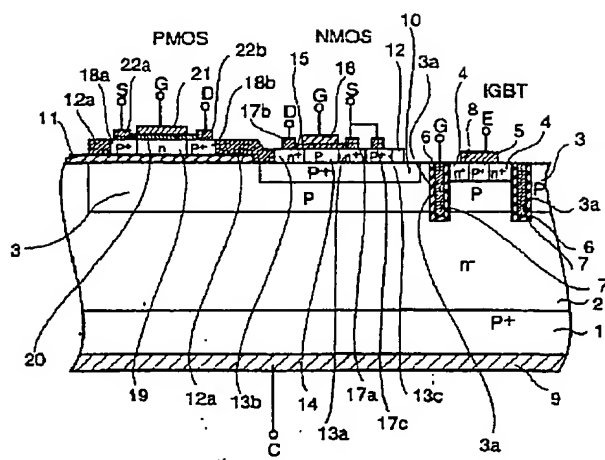
19

20

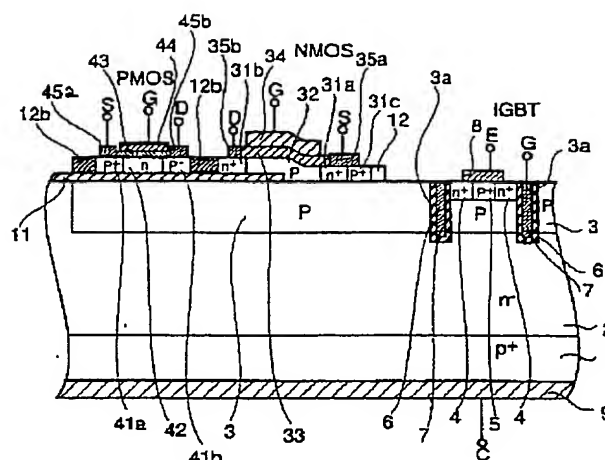
- 18 a n⁺ 型のソース層
18 b ドレイン層
19 チャネル領域
20 ゲート絶縁層

- 2 1 ゲート電極
2 2 a ソース電極
2 2 b ドレイン電極

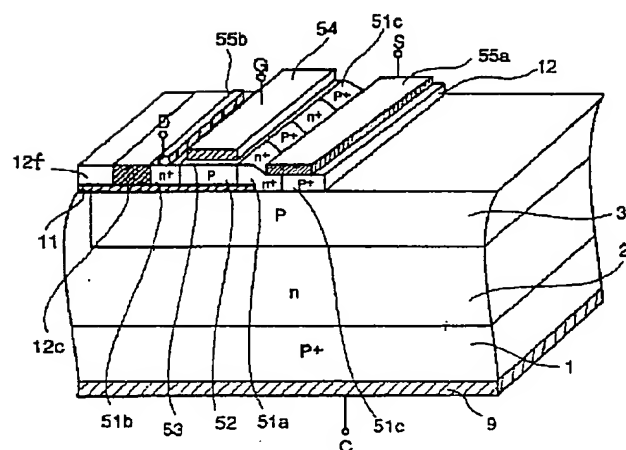
【图 1】



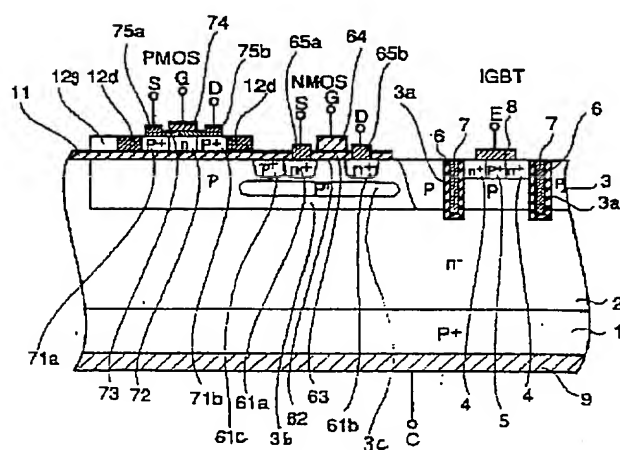
【図 2】



【图 3】



【图 4】



【図 6】

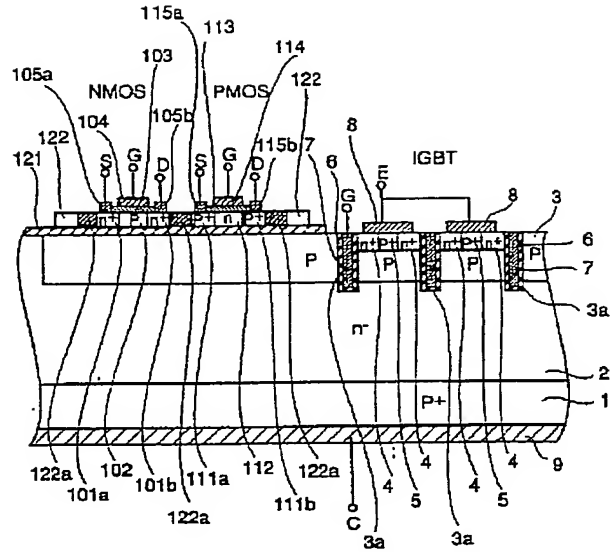


Figure 1 consists of two graphs, (a) and (b), illustrating the relationship between current (電流) and voltage (電圧).

Graph (a) shows three curves starting from the origin (0,0) and increasing with increasing slope, representing non-linear resistors. The vertical axis is labeled '電流' (Current) and the horizontal axis is labeled '電圧' (Voltage).

Graph (b) shows three curves starting from the origin (0,0) and increasing with decreasing slope, representing non-linear resistors. The vertical axis is labeled '電流' (Current) and the horizontal axis is labeled '電圧' (Voltage).

フロントページの続き

(51)Int.Cl.⁷

識別記号

F I

タームコード (参考)

H O 1 L 27/092

H O 1 L 29/78

6 1 3 A

29/78

6 5 3 A

29/786

6 5 5 A

6 5 6 D

6 5 7 C

F ターム (参考) 5F038 BH04 BH12 EZ14 EZ20
 5F040 DA00 DA06 DA23 DB01 DB03
 DB06 DC01 EB12 EB14 EC19
 EMO0 EMO1 EMO3 EMO4 FC07
 5F048 AA03 AA07 AC01 AC03 AC10
 BA02 BA12 BA20 BB01 BB05
 BC11 BC16 BC18 BC19 BD09
 BE08 BG06 BH01 CB07 CC04
 CC06 CC15 CC16 CC18
 5F110 AA06 AA08 BB04 CC02 DD05
 DD13 FF02 GG02 GG13 NN71
 PP01 PP10

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